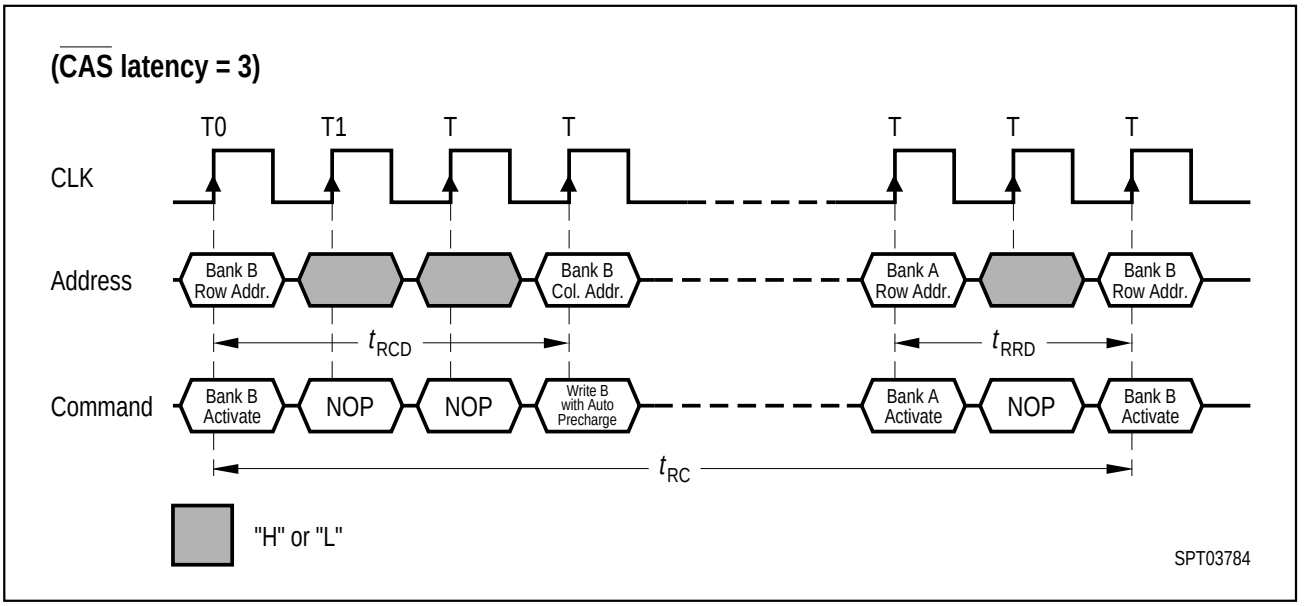
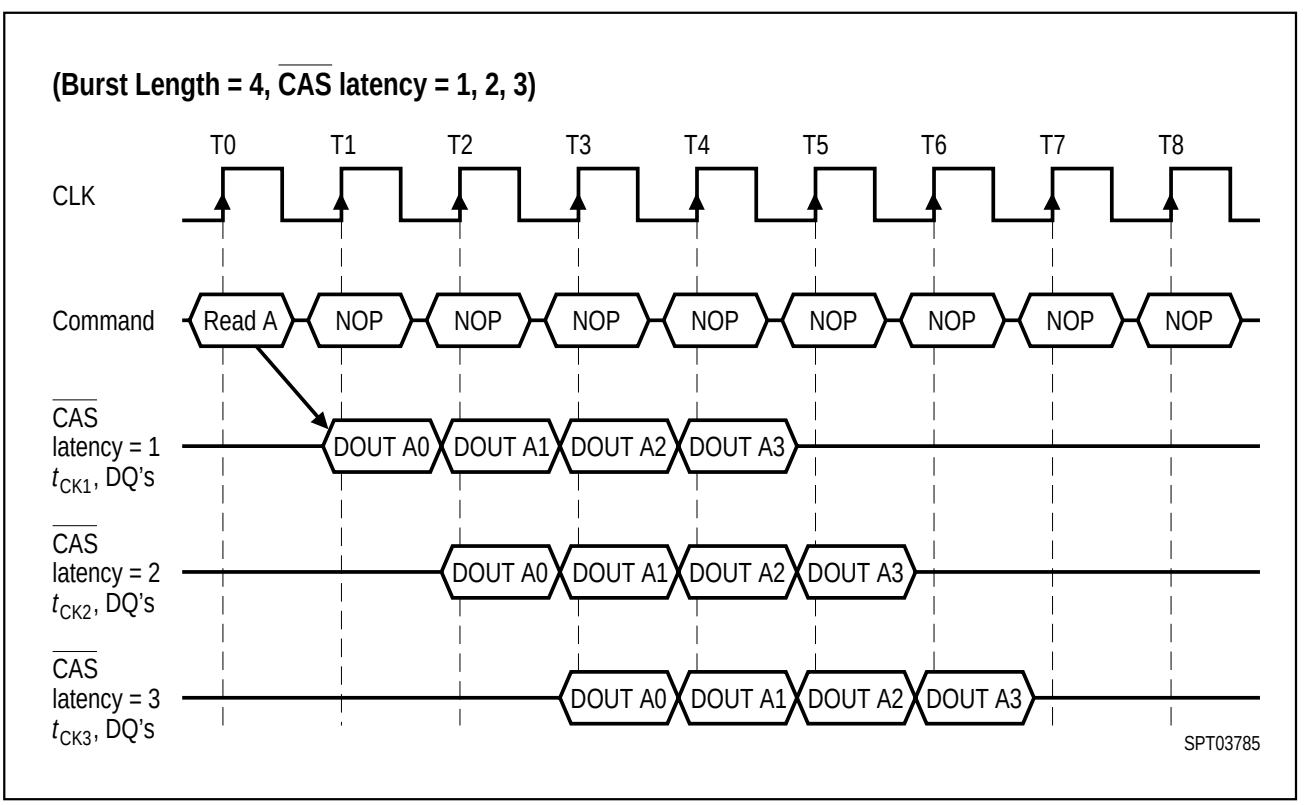
Timing Diagrams

Timing Diagrams (cont'd)

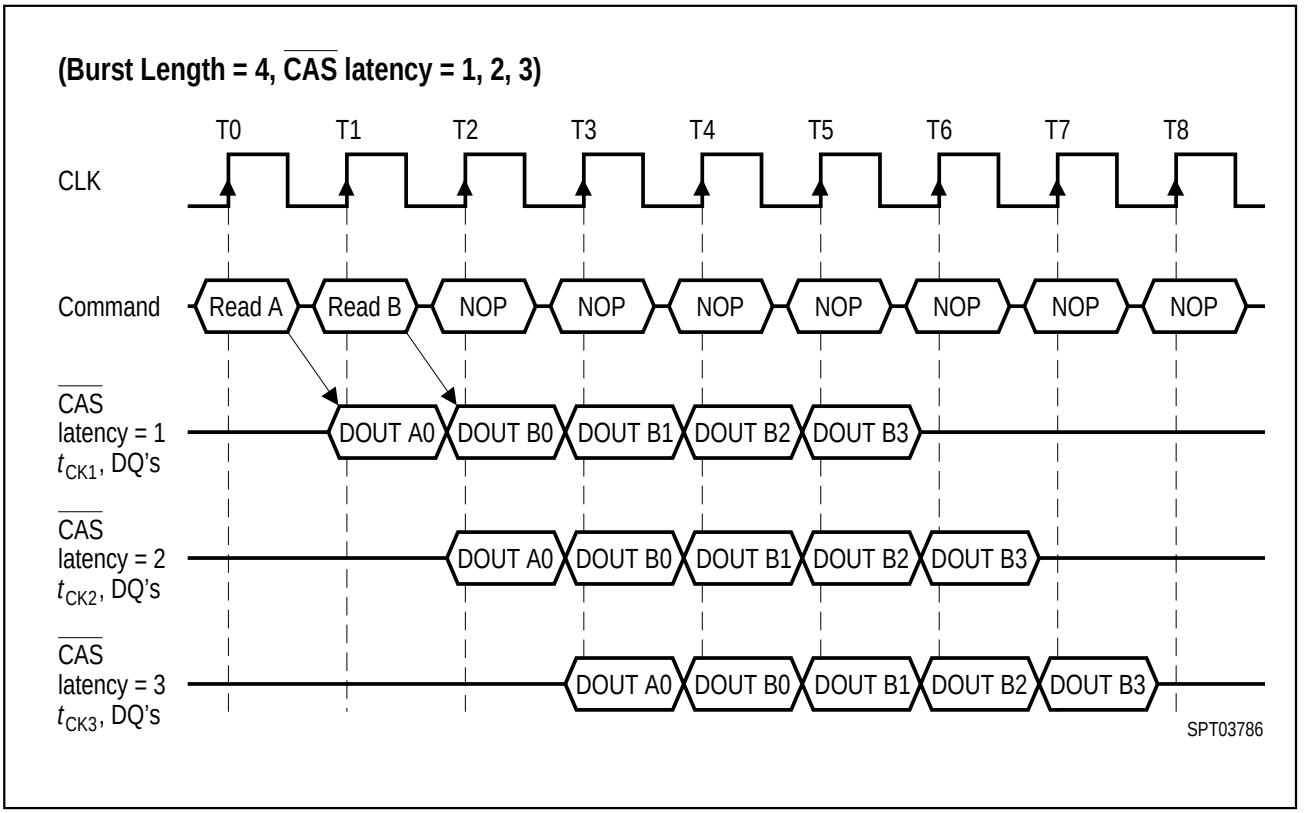
1. Bank Activate Command Cycle



2. Burst Read Operation

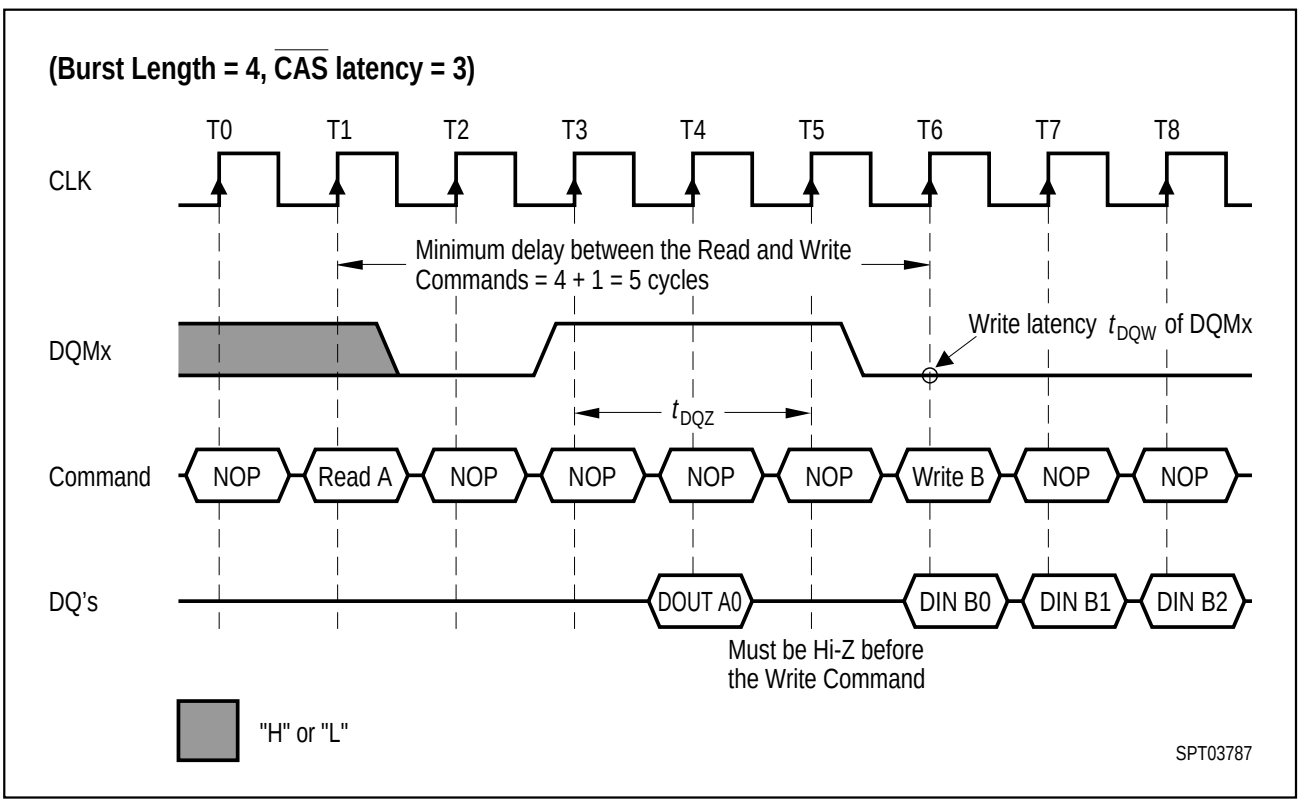


3. Read Interrupted by a Read

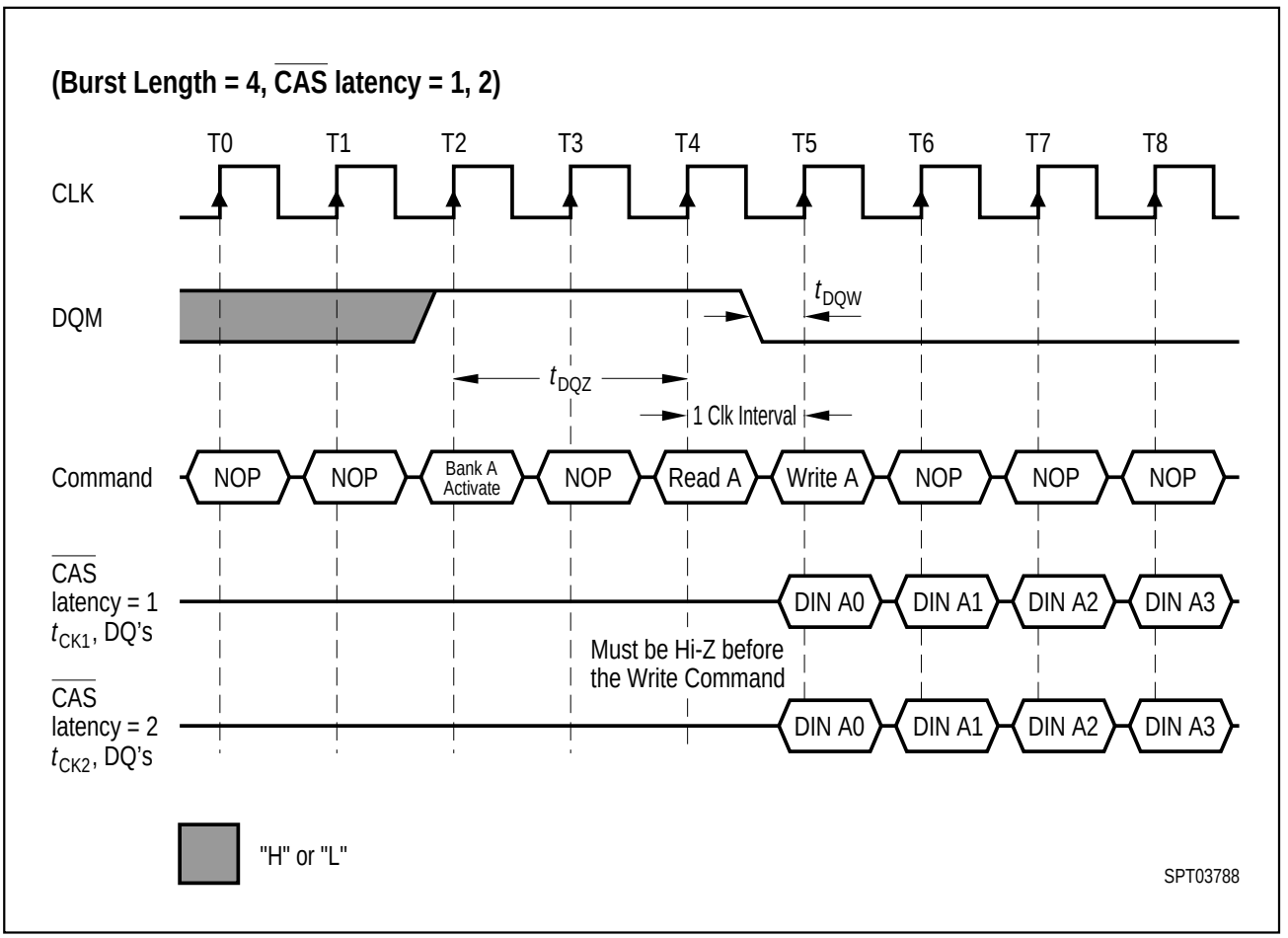


4. Read to Write Interval

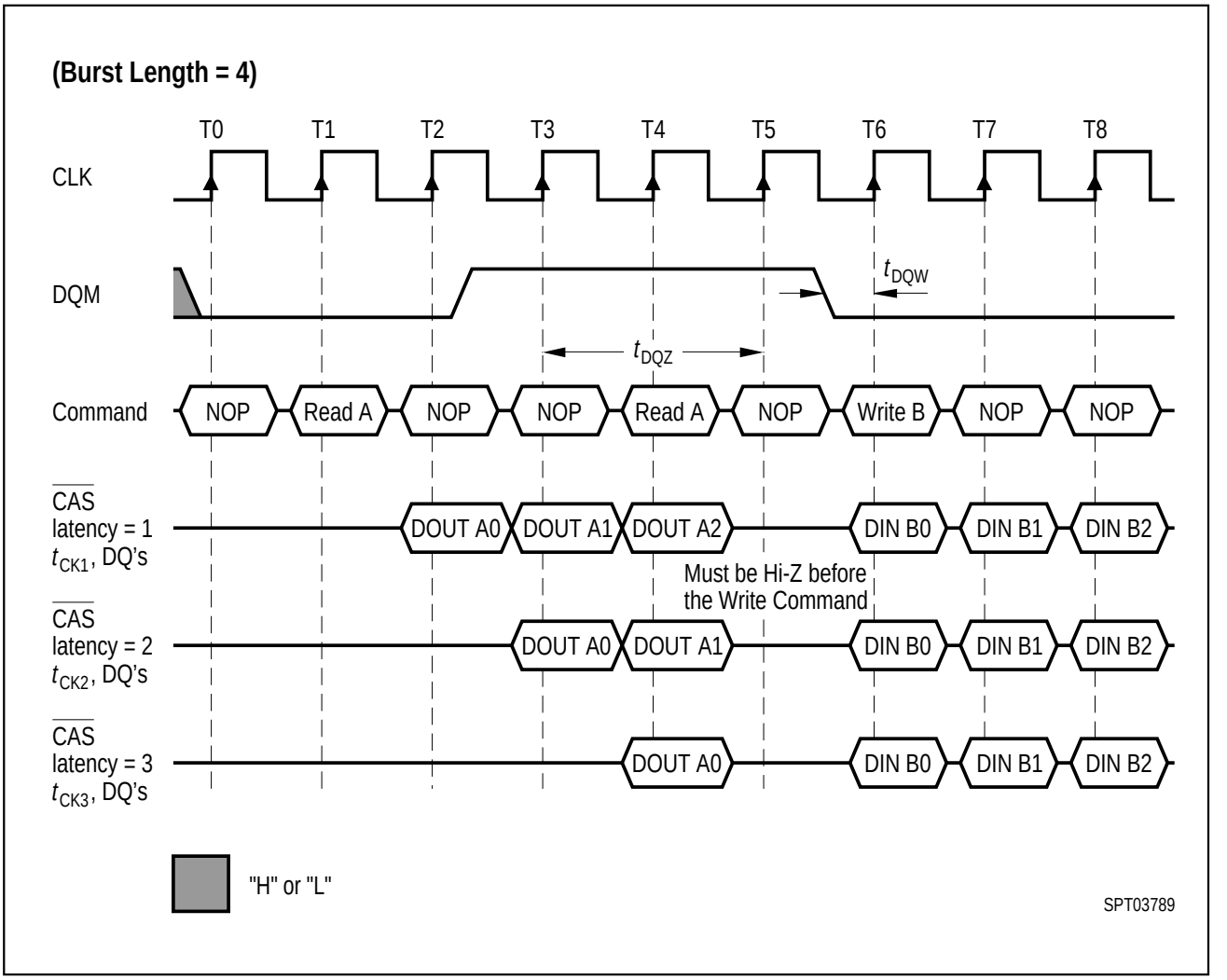
4.1. Read to Write Interval



4.2. Minimum Read to Write Interval

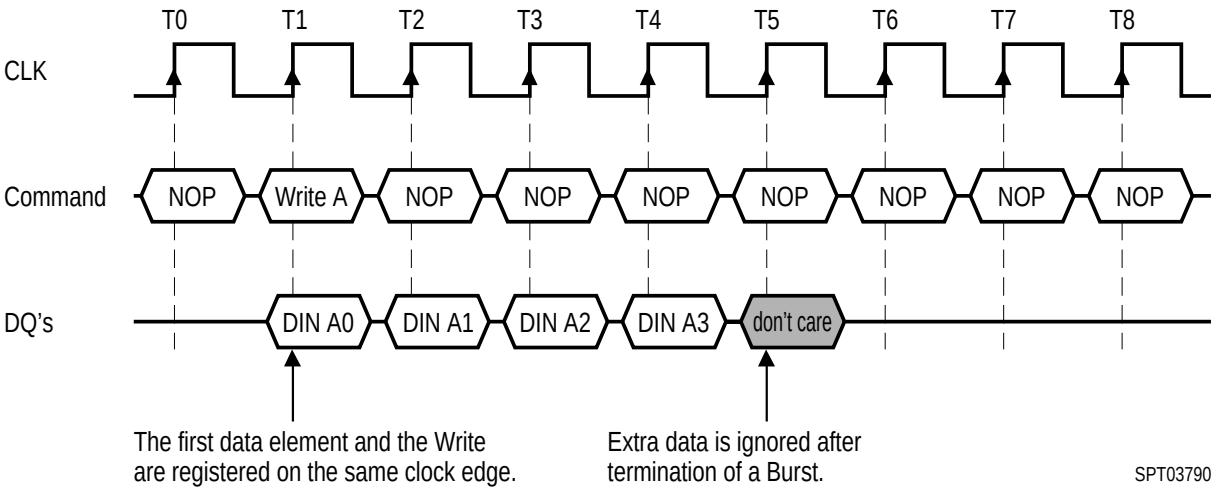


4.3. Non-Minimum Read to Write Interval



5. Burst Write Operation

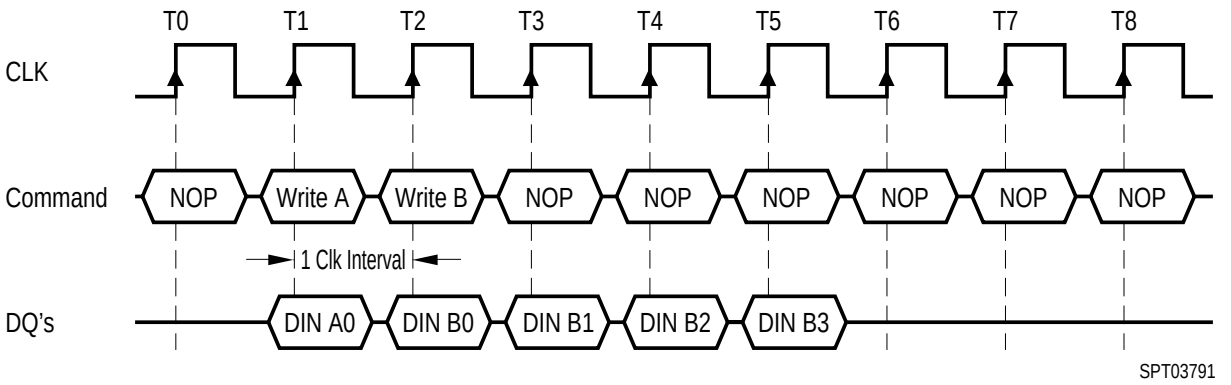
(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)



6. Write and Read Interrupt

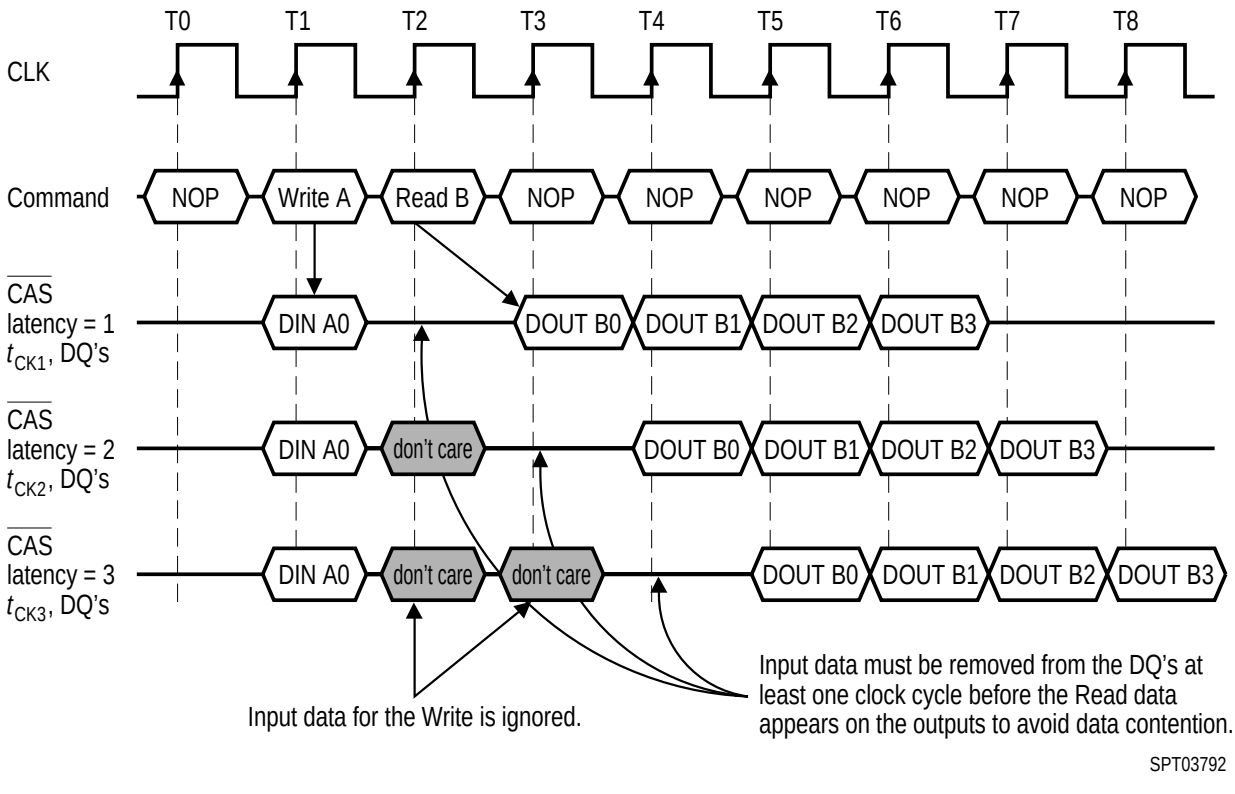
6.1. Write Interrupted by a Write

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 2, 3)



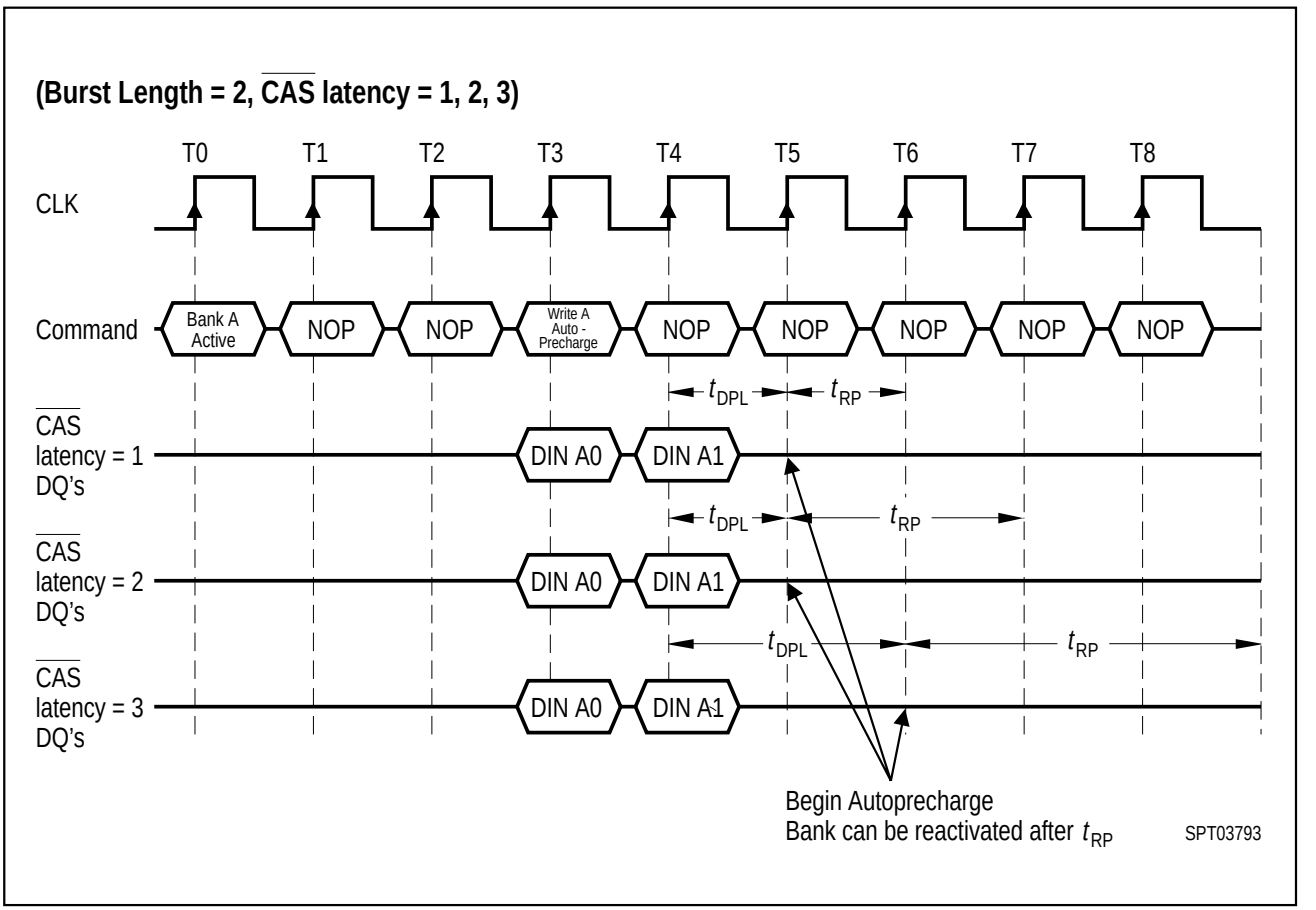
6.2. Write Interrupted by a Read

(Burst Length = 4, $\overline{\text{CAS}}$ latency = 1, 2, 3)

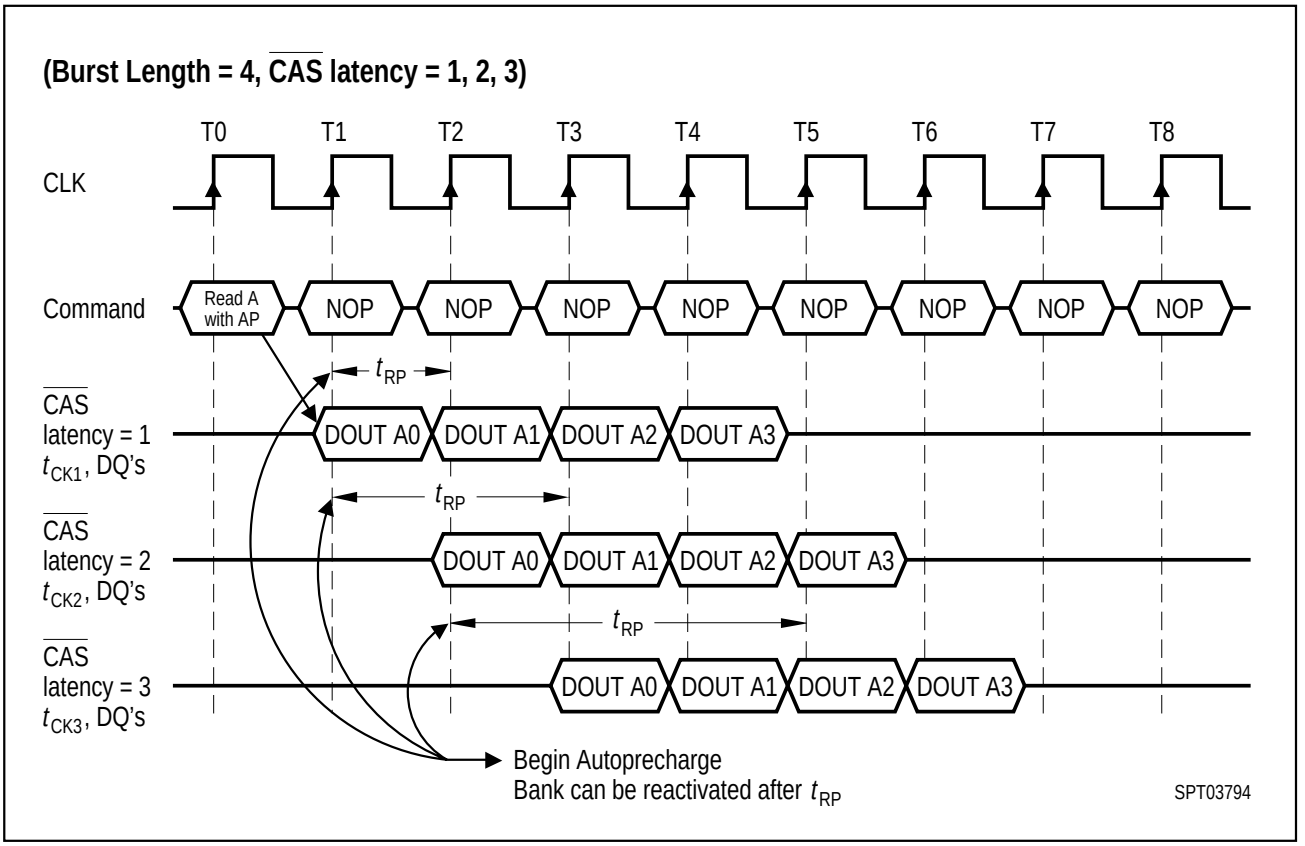


7. Burst Write and Read with Auto Precharge

7.1. Burst Write with Auto Precharge

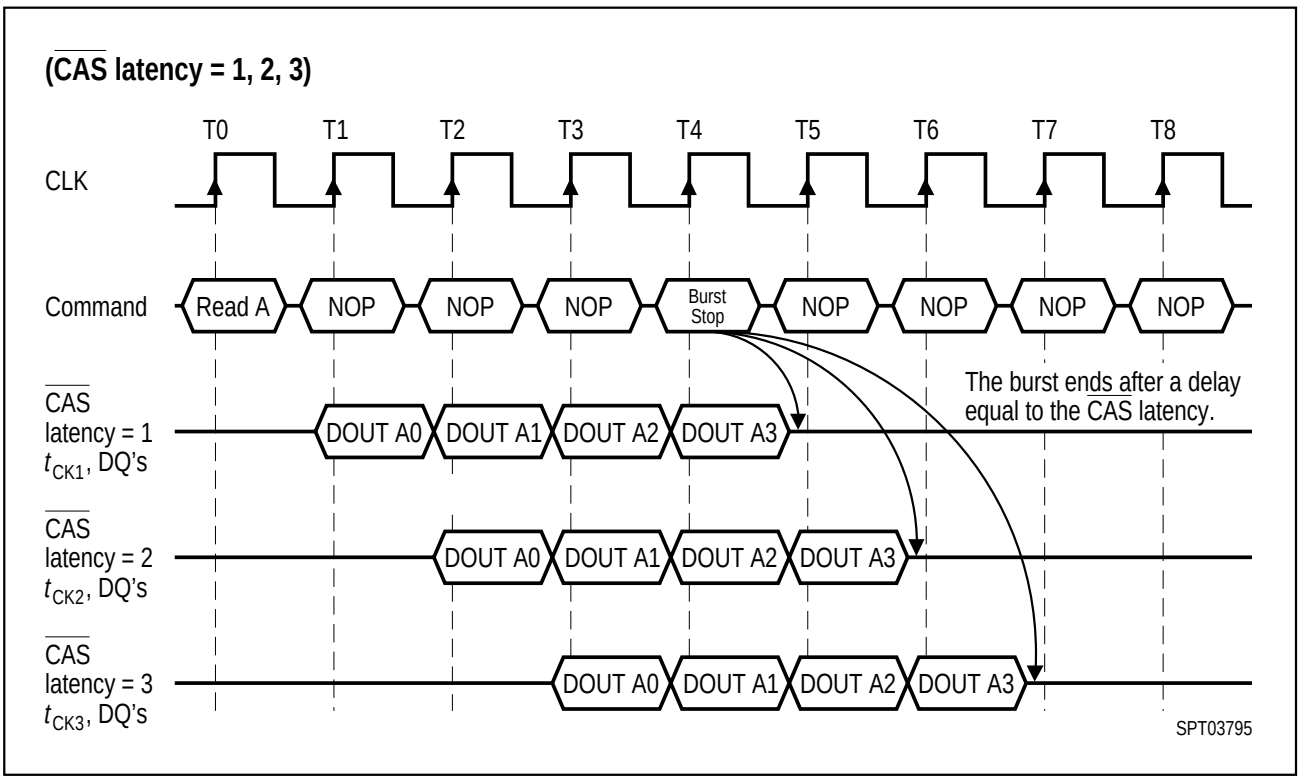


7.2. Burst Read with Auto Precharge

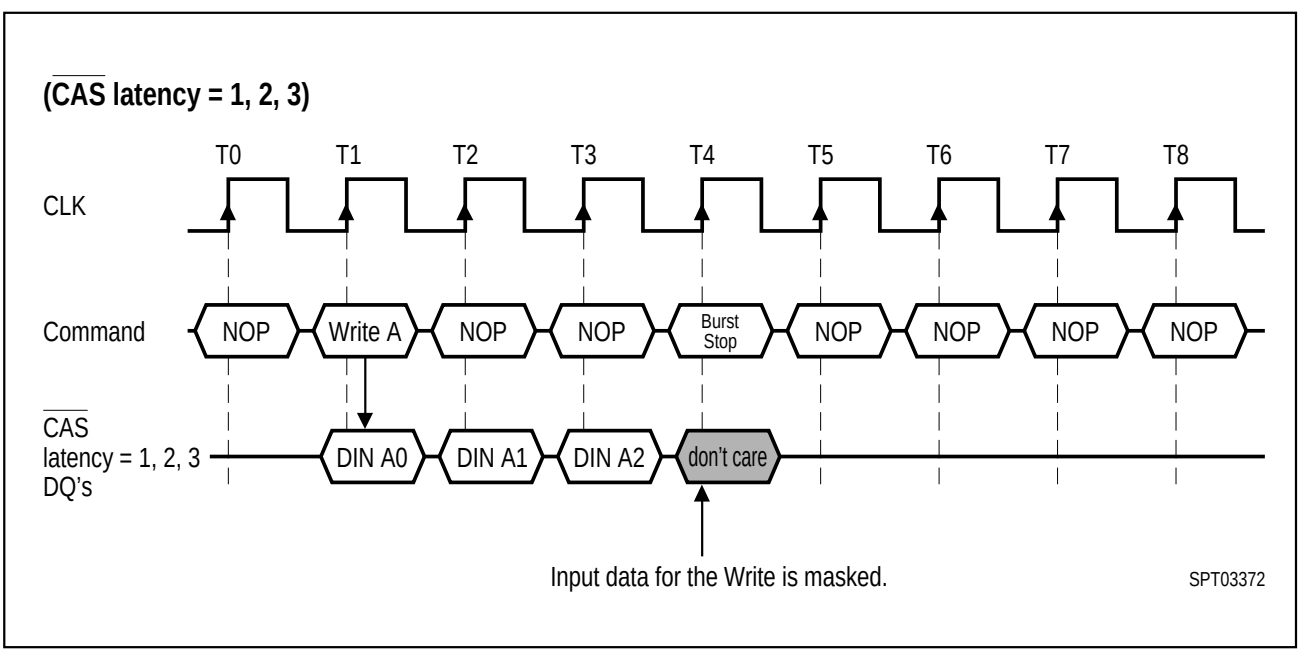


8. Burst Termination

8.1. Termination of a Full Page Burst Read Operation

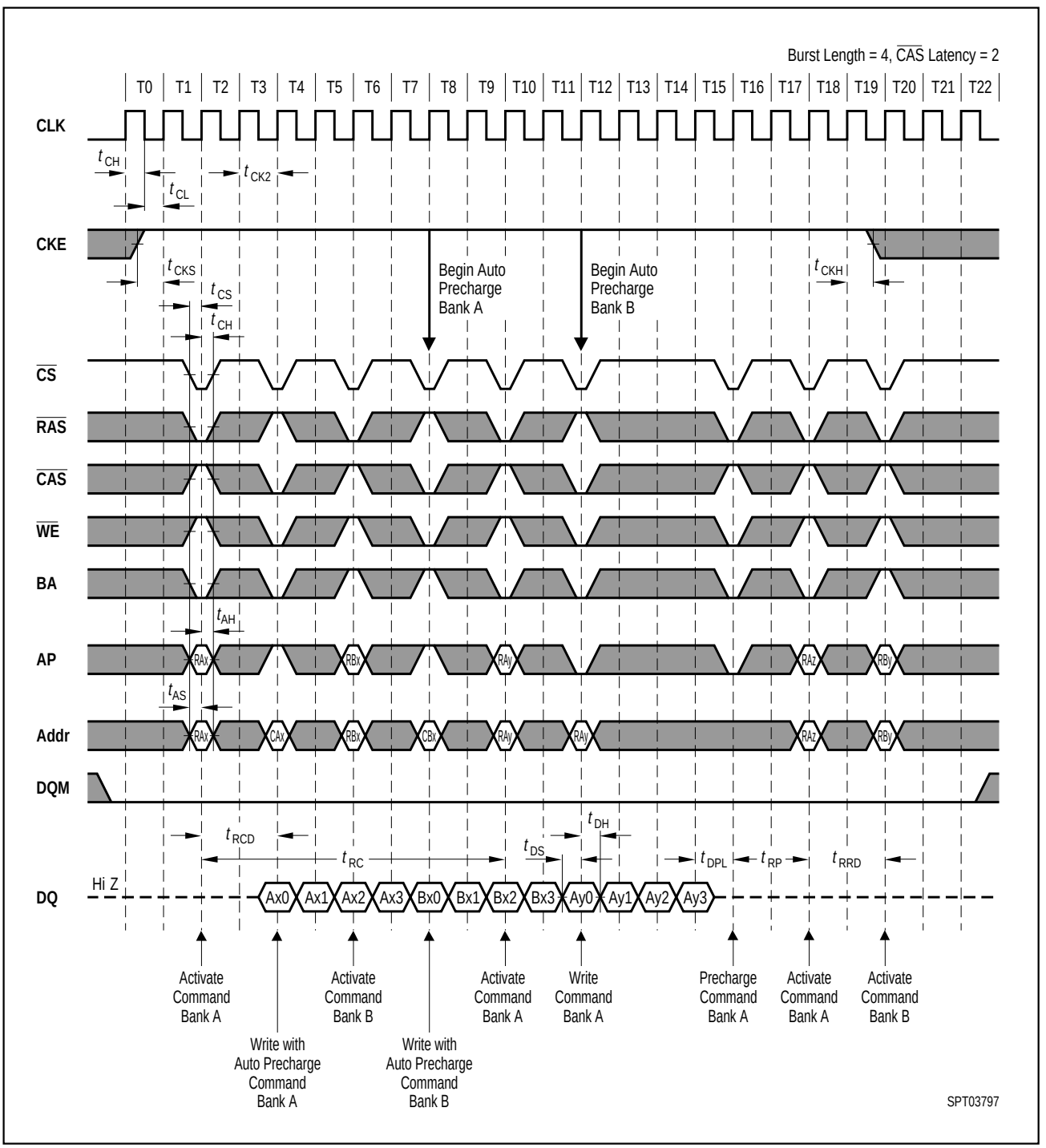


8.2. Termination of a Full Page Burst Write Operation

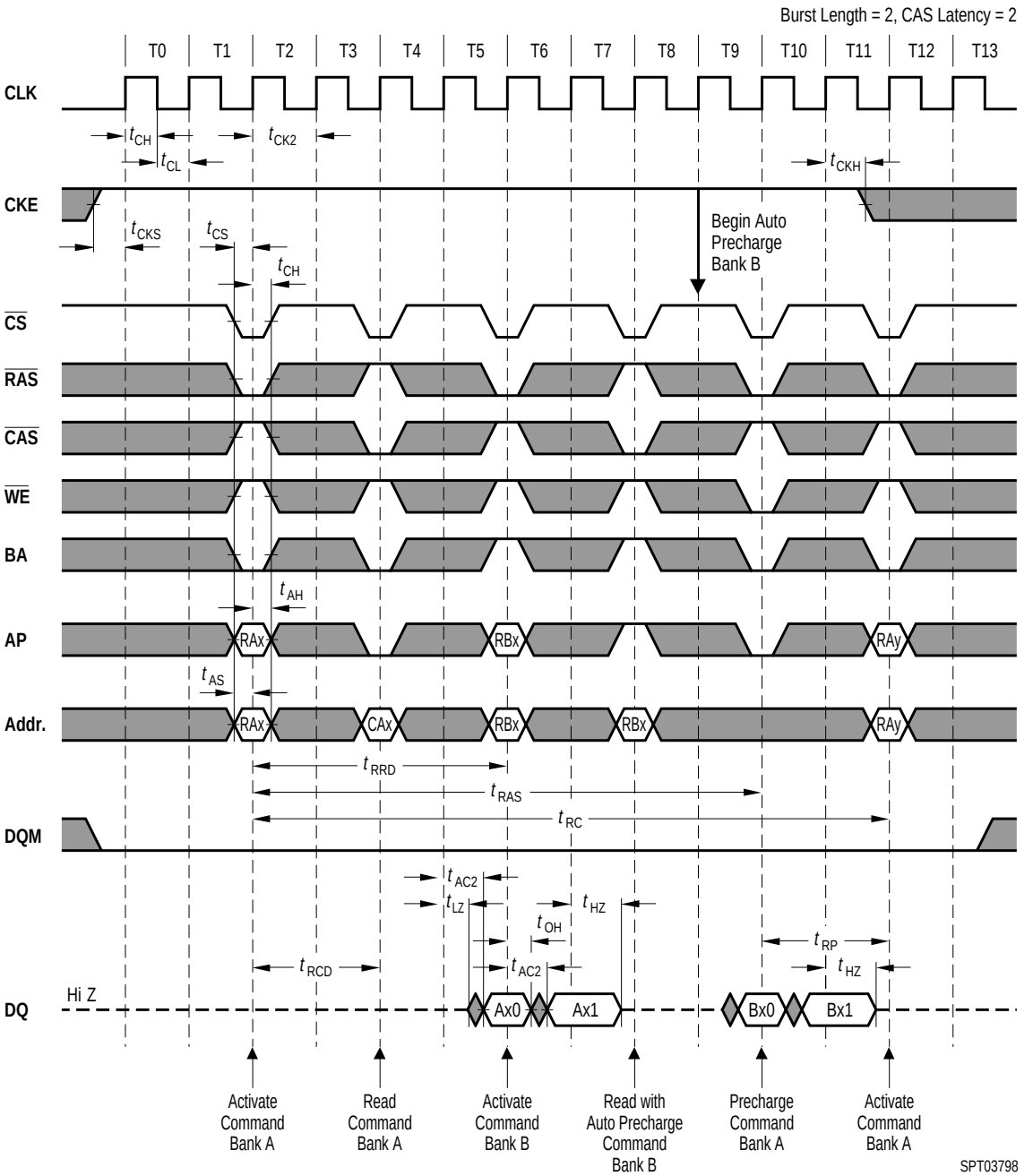


9. AC Parameters

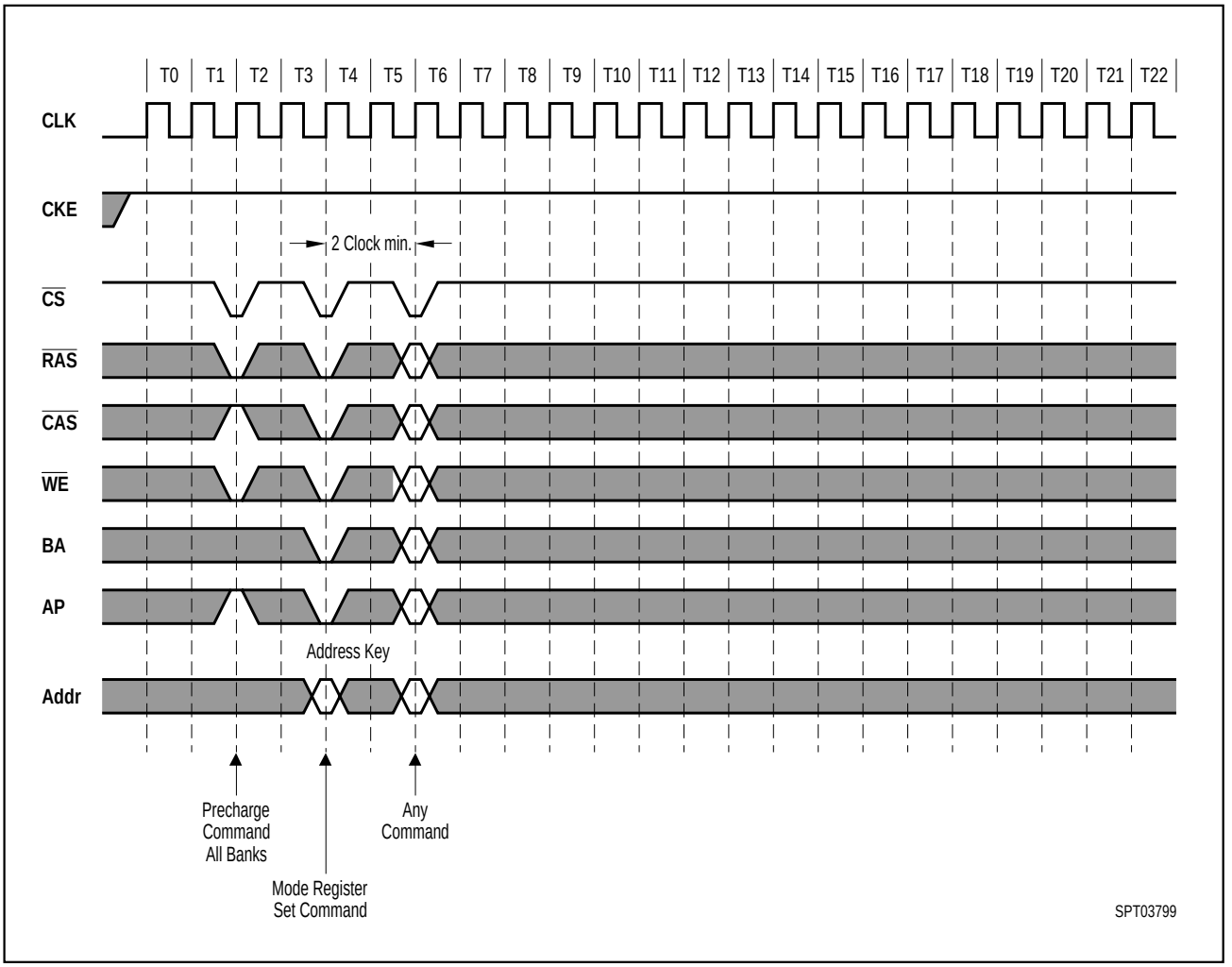
9.1. AC Parameters for Write Timing



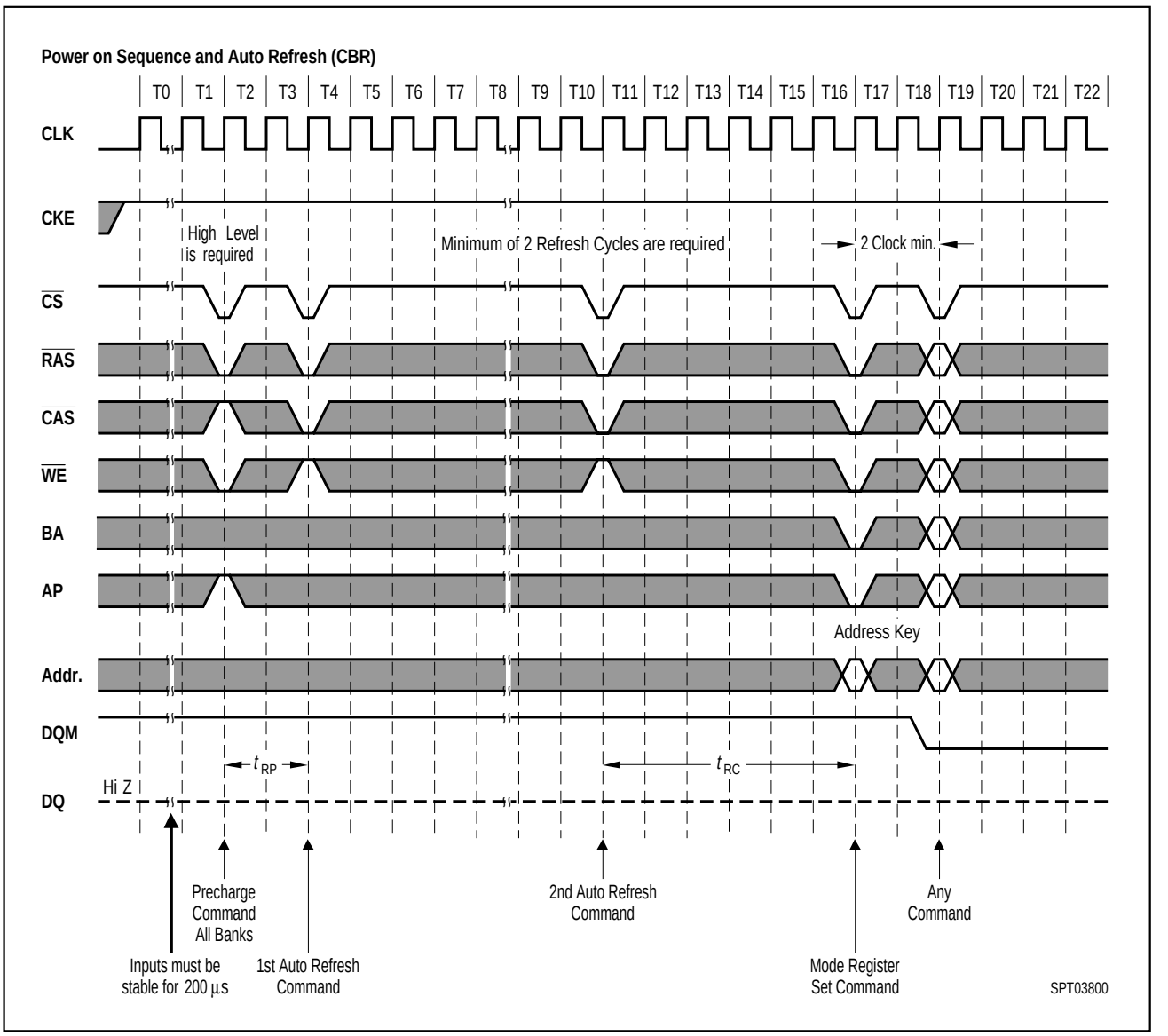
9.2. AC Parameters for Read Timing



10. Mode Register Set

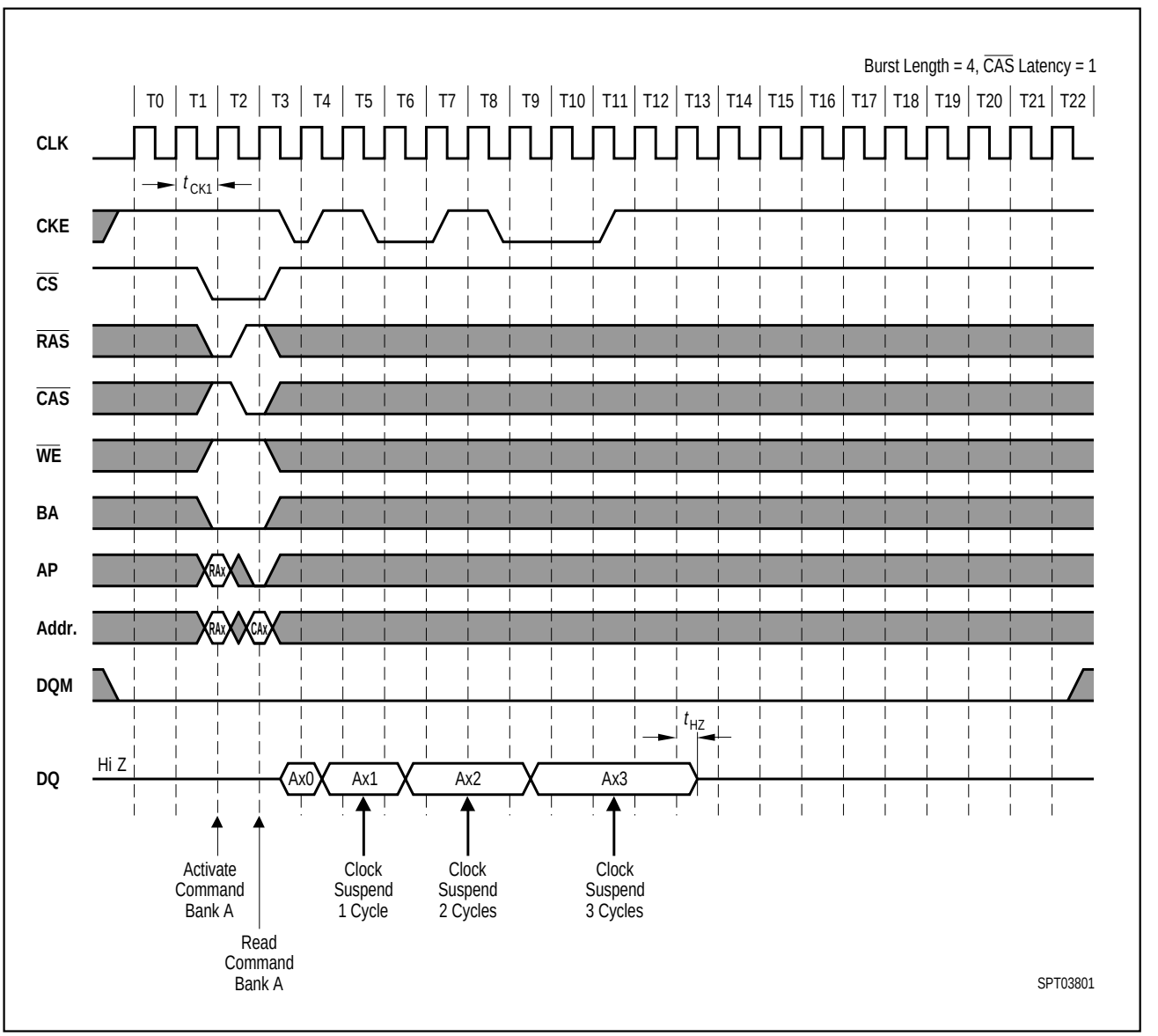


11. Power on Sequence and Auto Refresh (CBR)

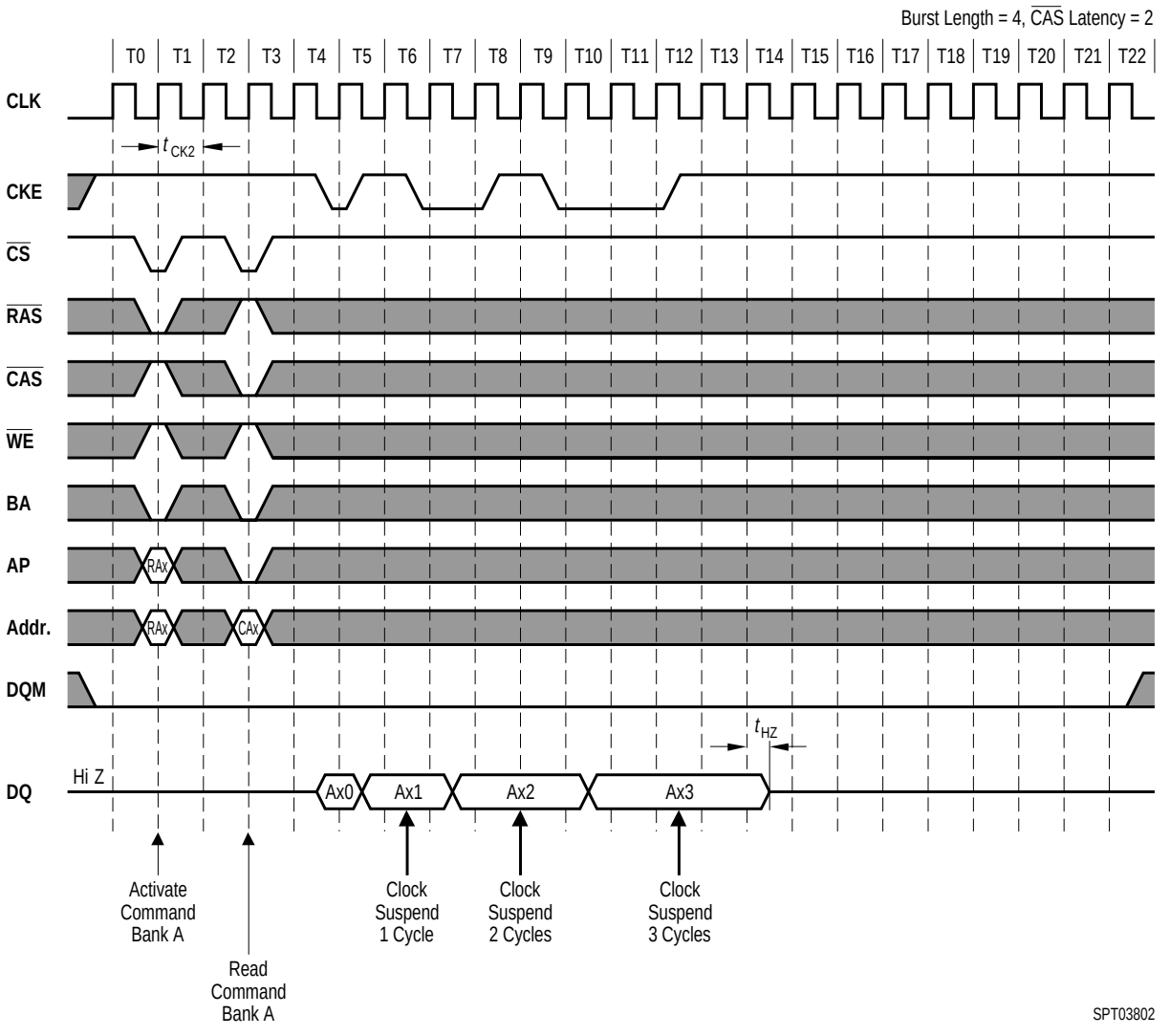


12. Clock Suspension (Using CKE)

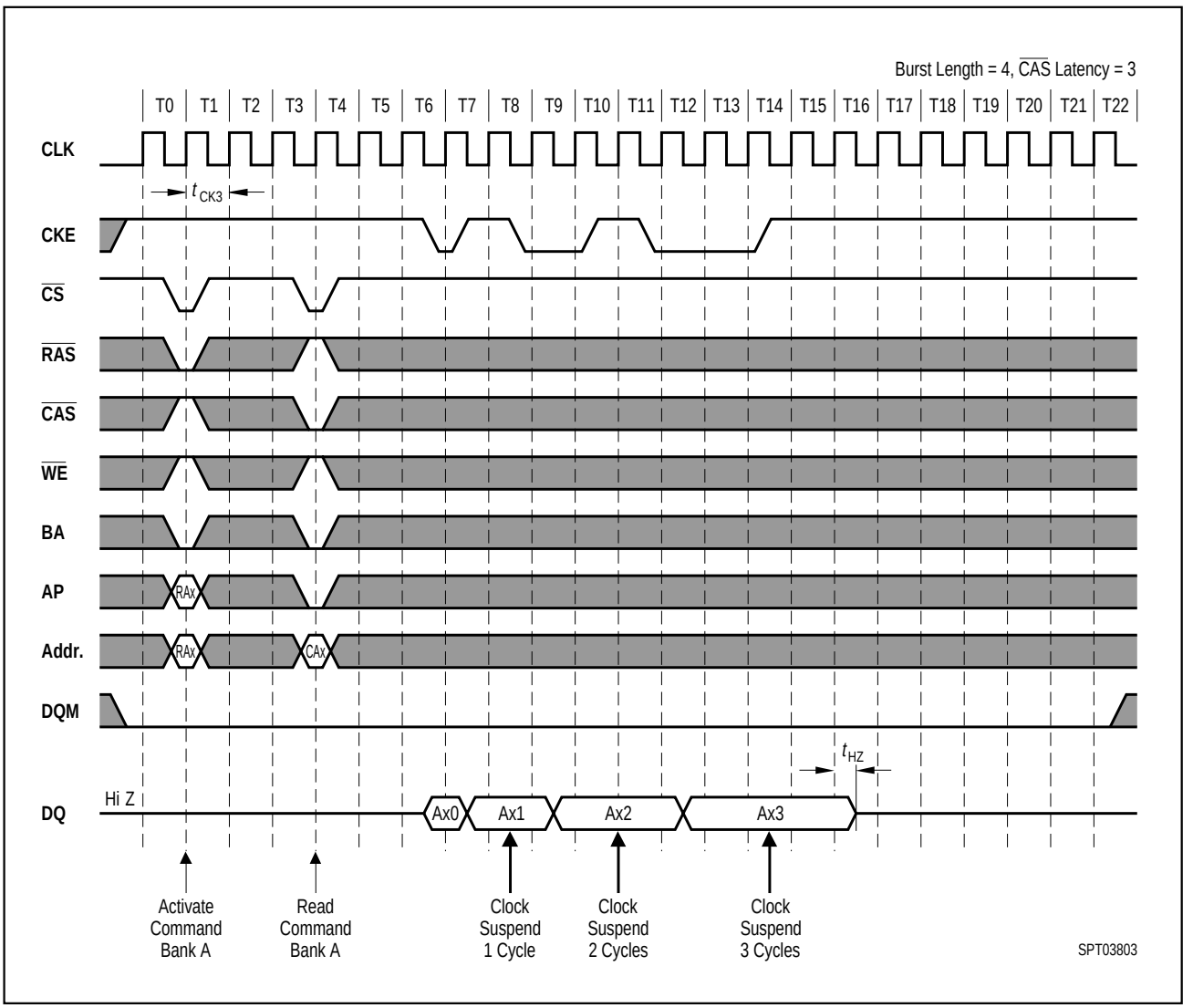
12.1. Clock Suspension During Burst Read $\overline{CAS}$ Latency = 1



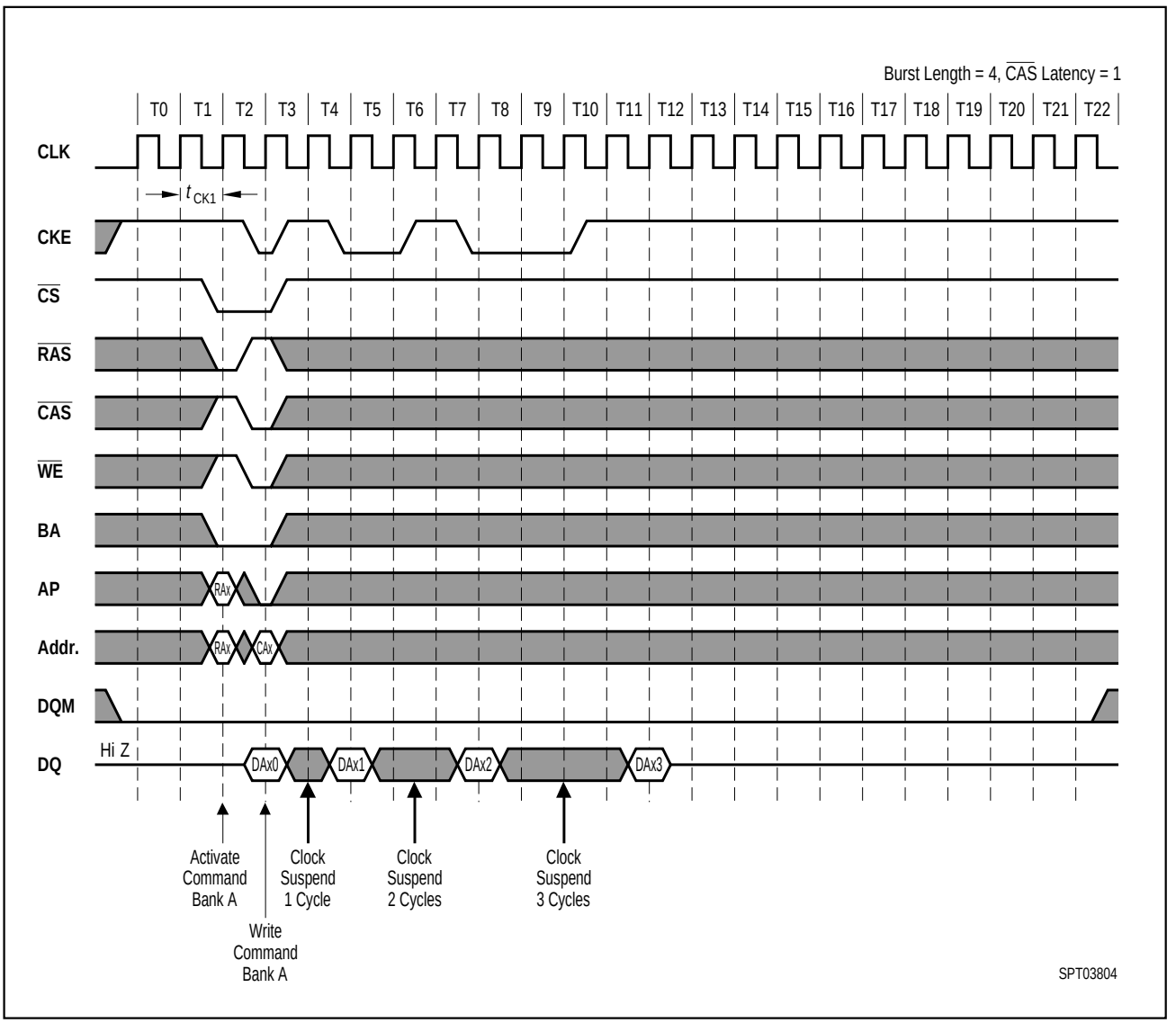
12.2. Clock Suspension During Burst Read $\overline{CAS}$ Latency = 2



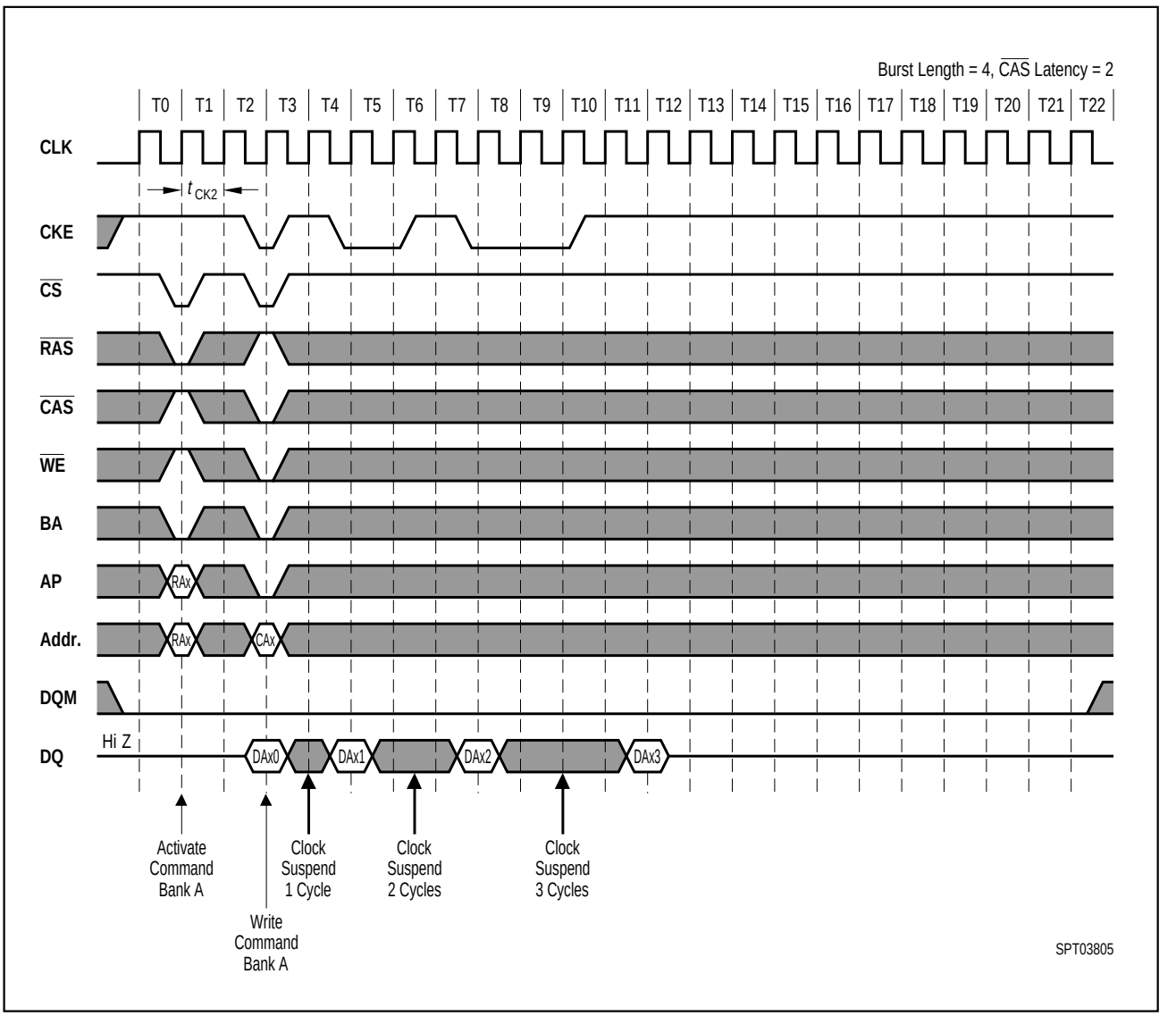
12.3. Clock Suspension During Burst Read $\overline{CAS}$ Latency = 3



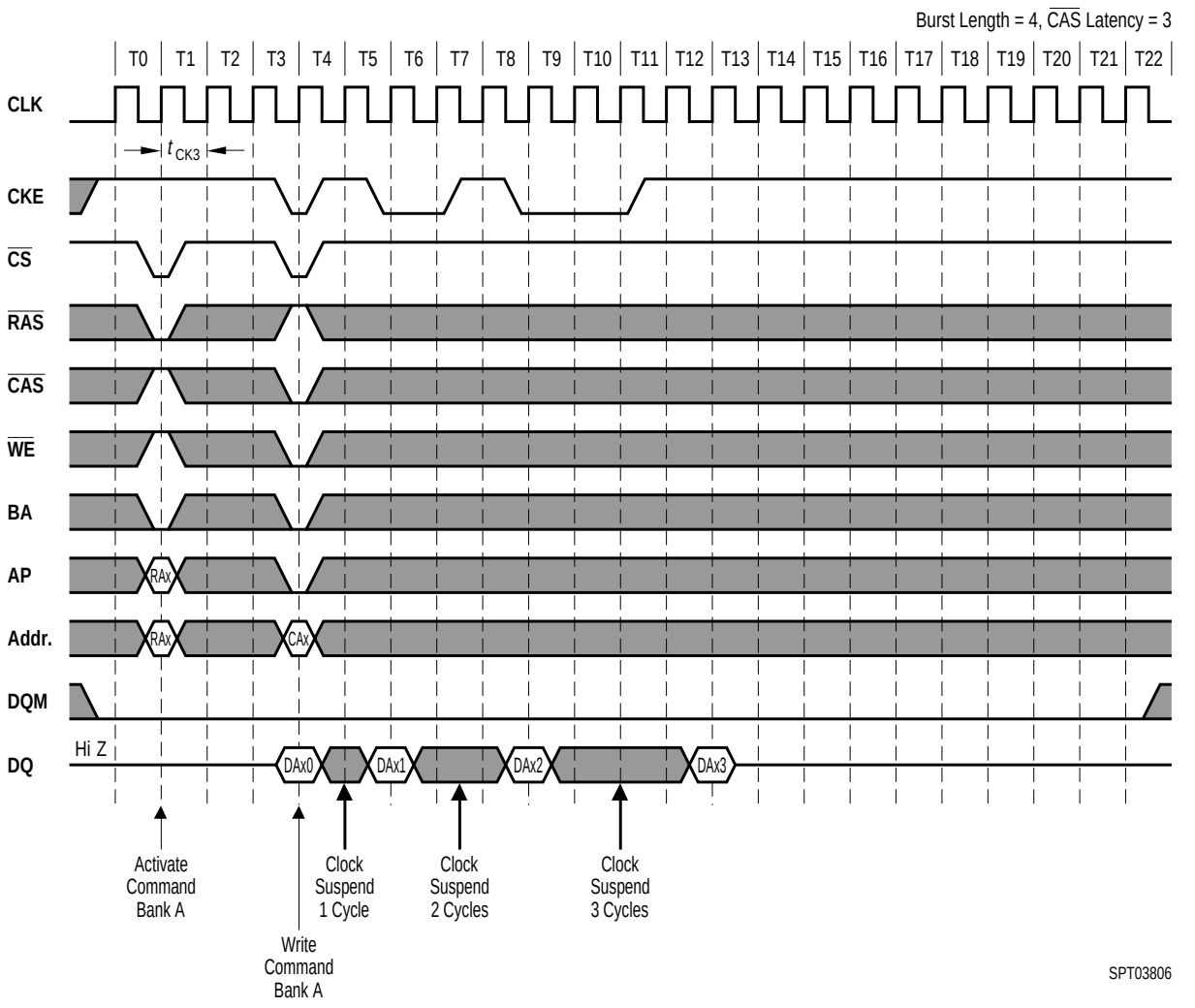
12.4. Clock Suspension During Burst Write $\overline{CAS}$ Latency = 1



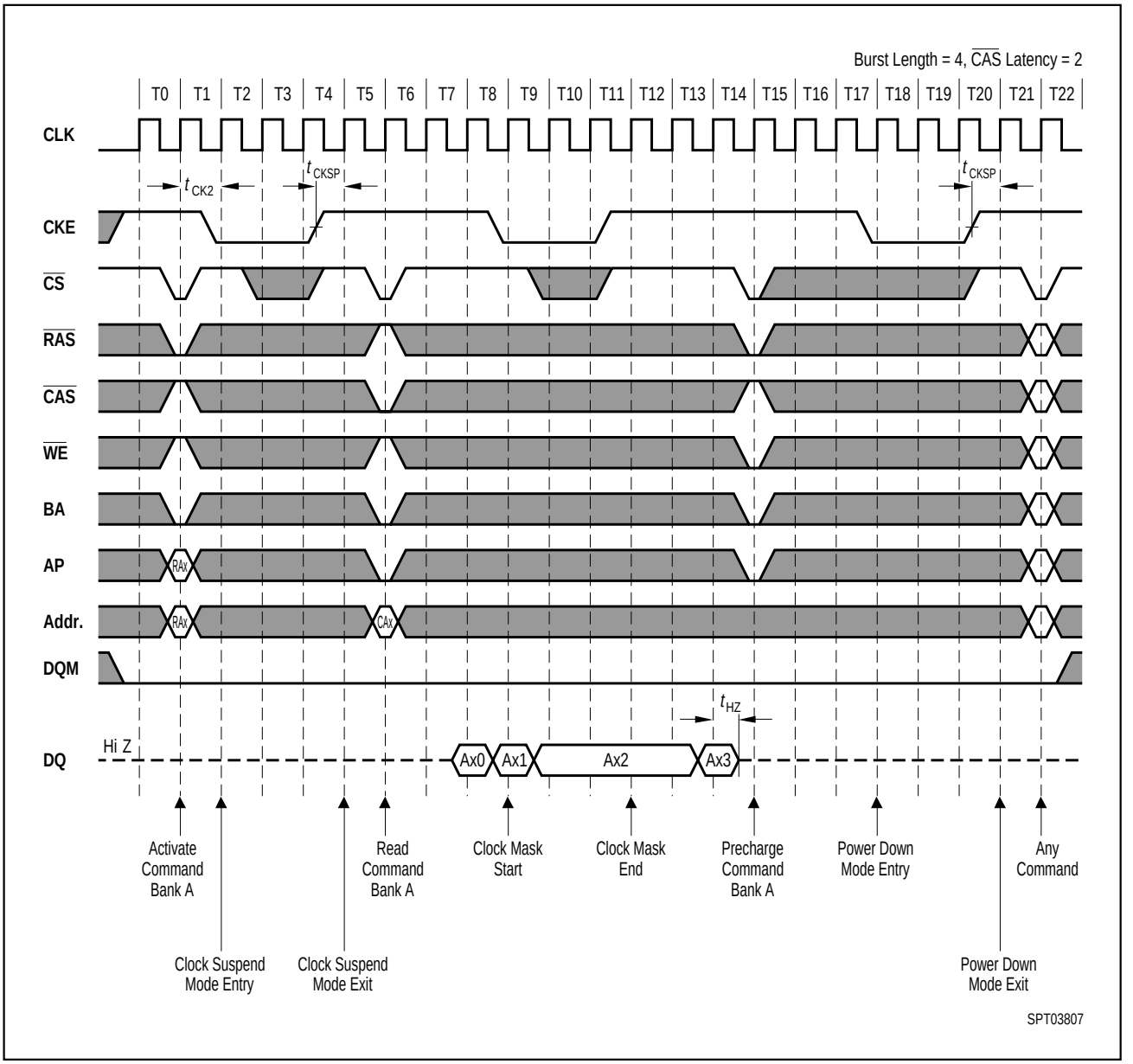
12.5. Clock Suspension During Burst Write $\overline{CAS}$ Latency = 2



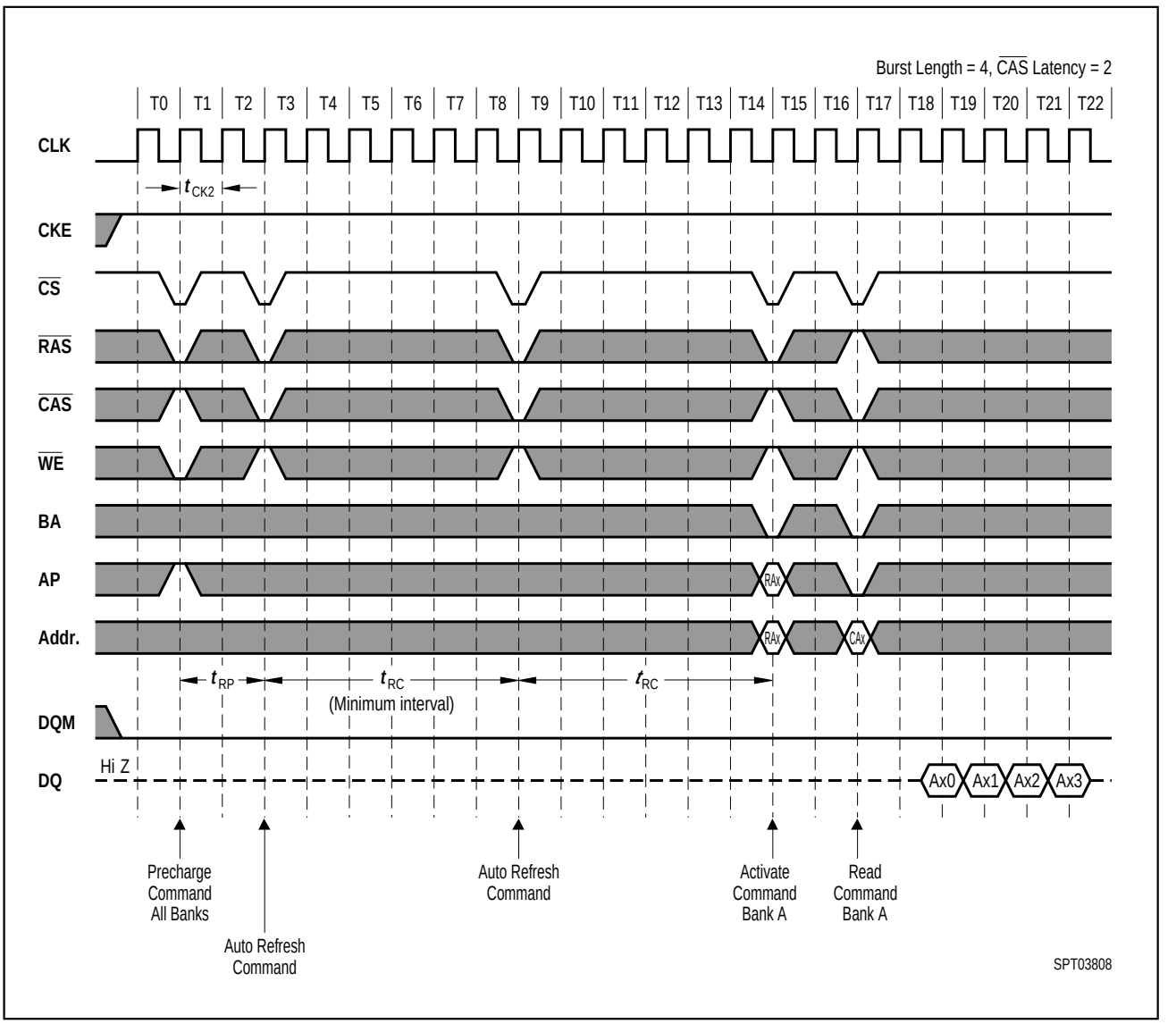
12.6. Clock Suspension During Burst Write $\overline{CAS}$ Latency = 3



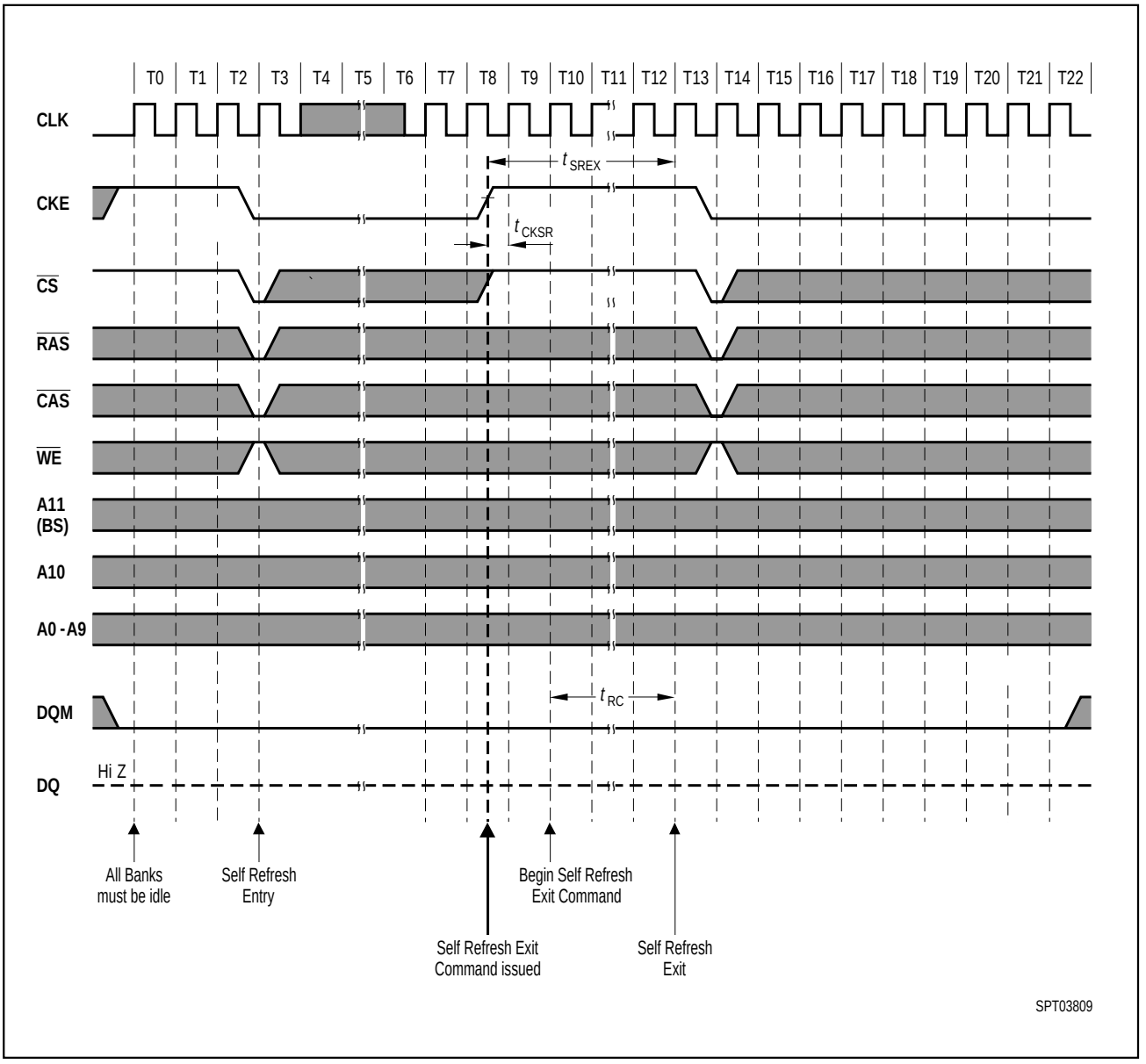
13. Power Down Mode and Clock Suspend



14. Auto Refresh (CBR)

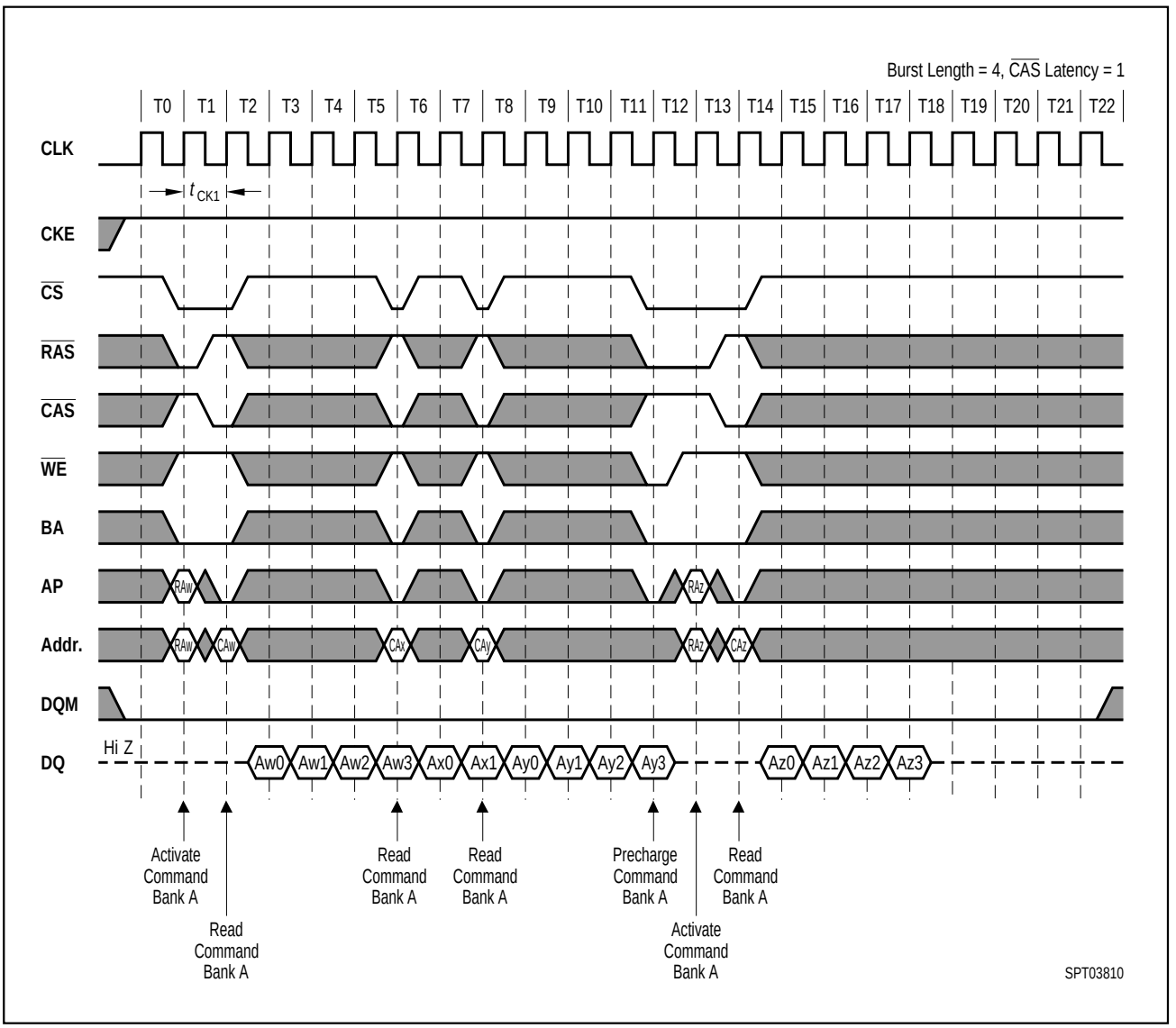


15. Self Refresh (Entry and Exit)

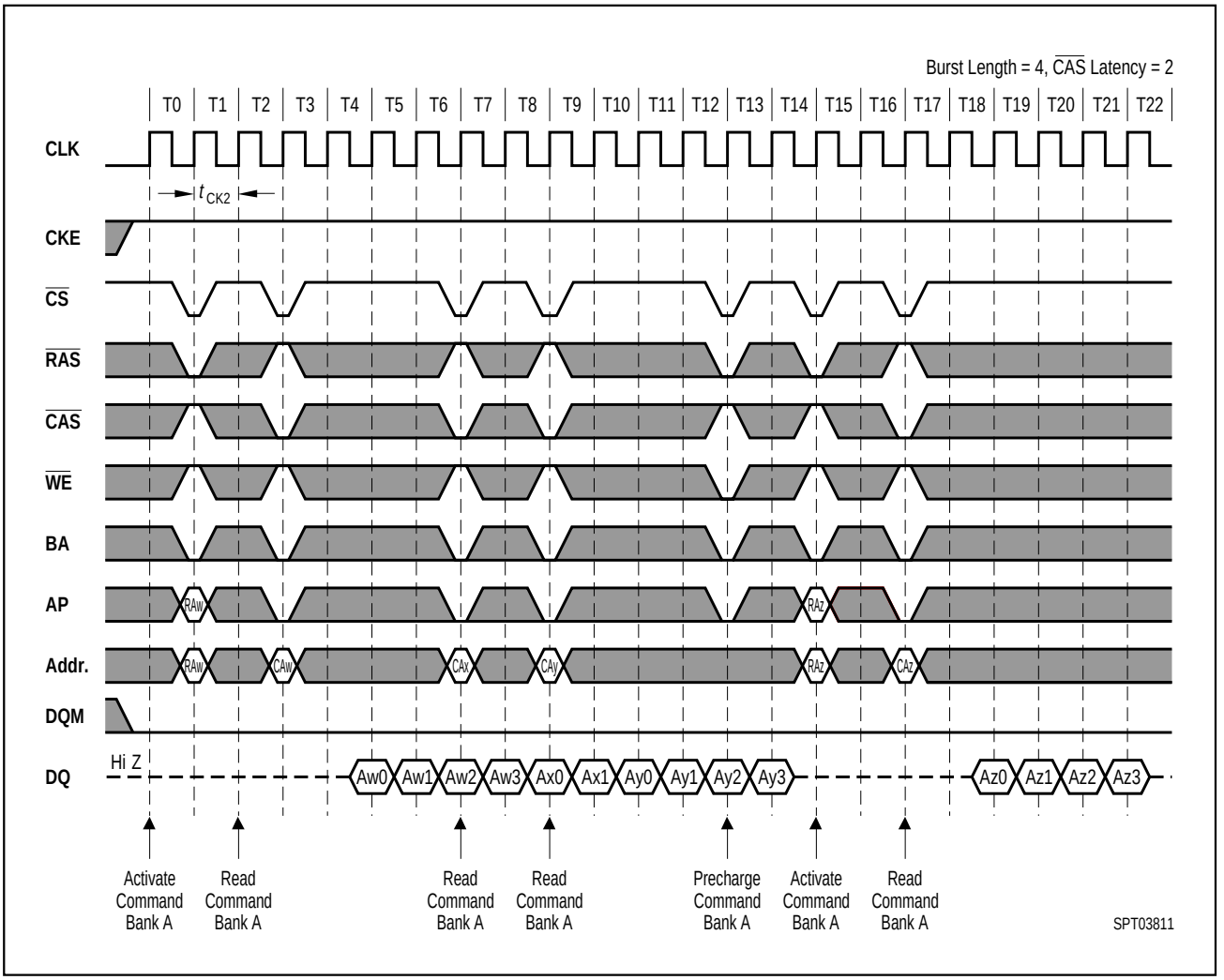


16. Random Column Read (Page within same Bank)

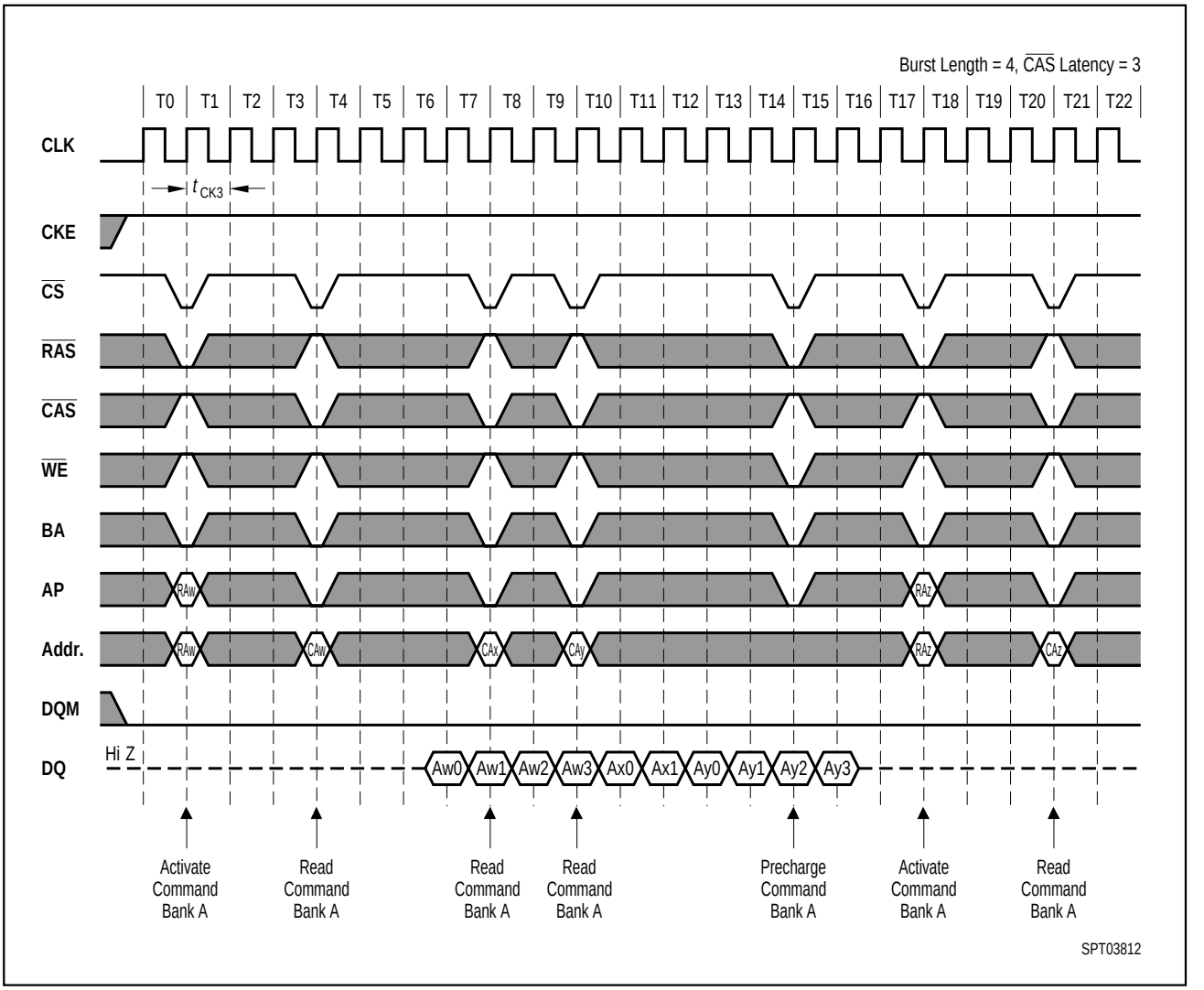
16.1. $\overline{CAS}$ Latency = 1



16.2. $\overline{\text{CAS}}$ Latency = 2

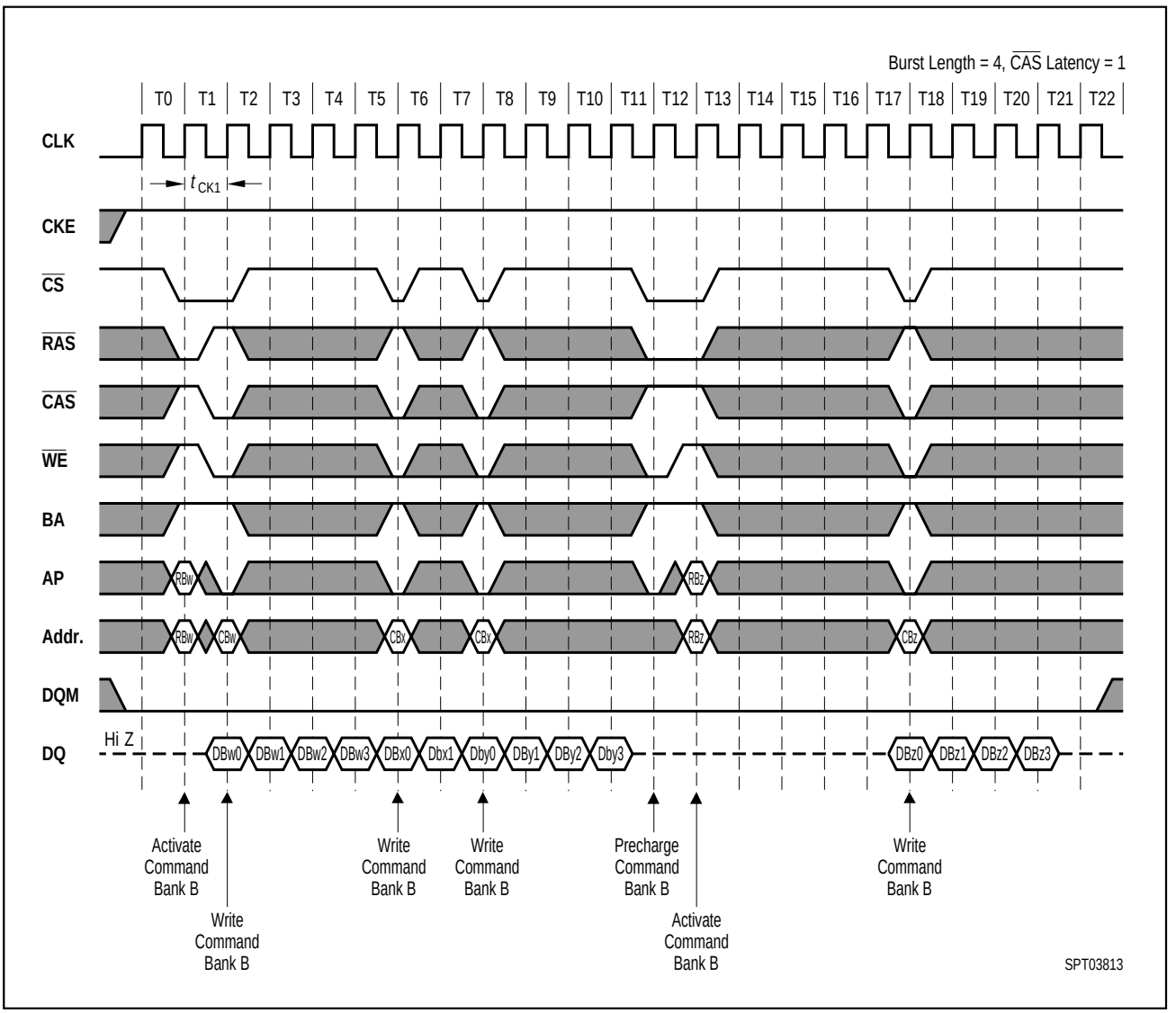


16.3. $\overline{\text{CAS}}$ Latency = 3

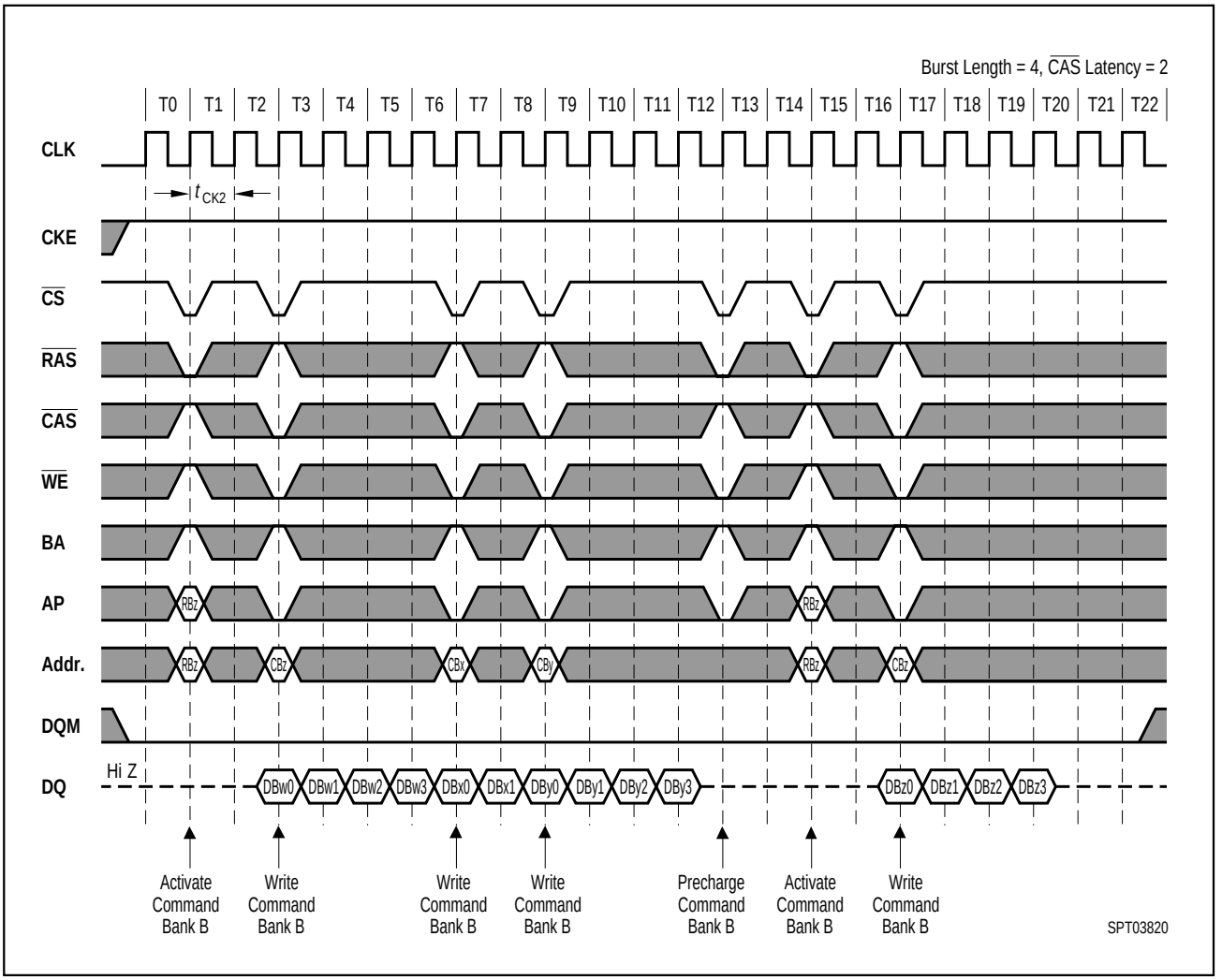


17. Random Column Write (Page within same Bank)

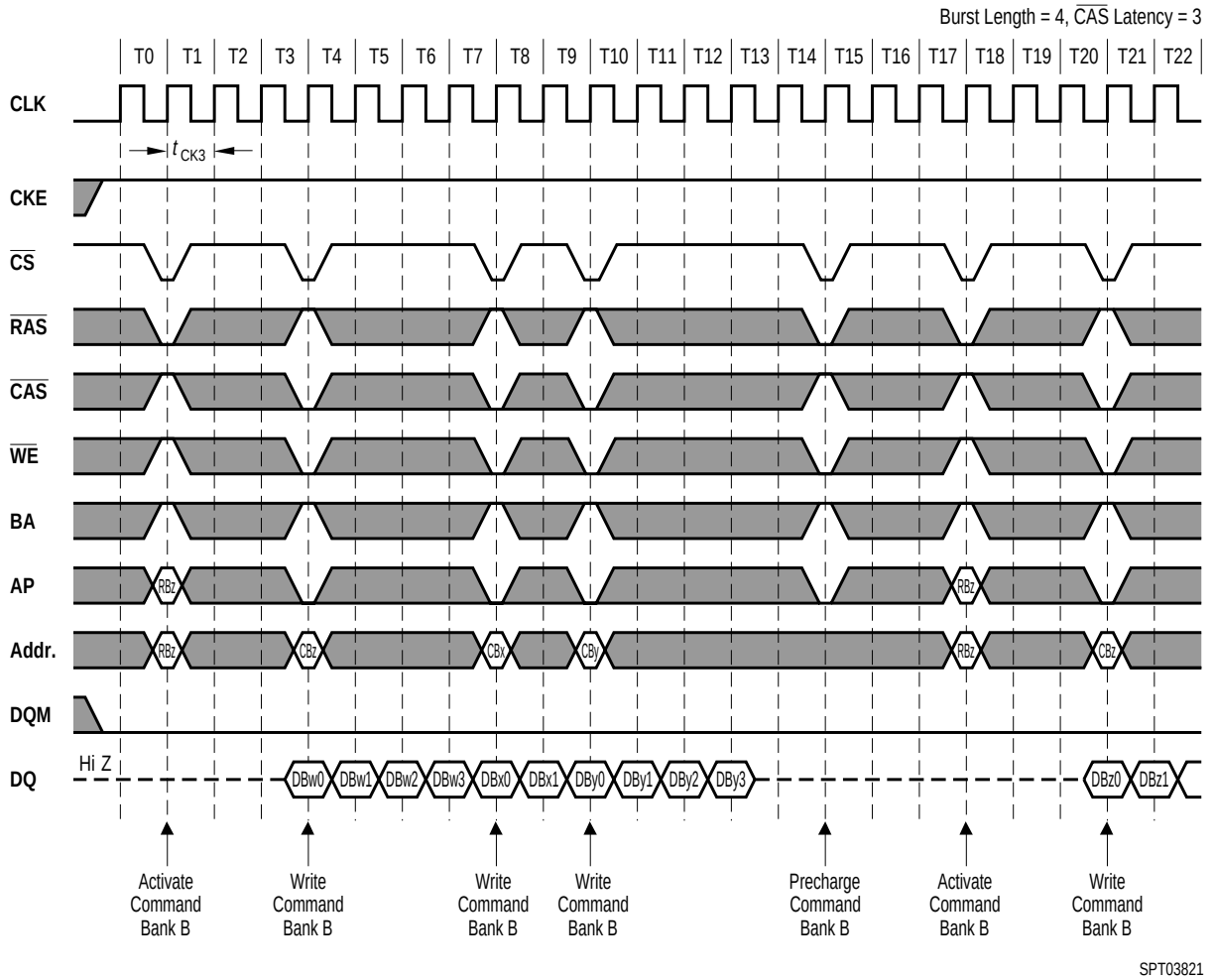
17.1. $\overline{CAS}$ Latency = 1



17.2. $\overline{\text{CAS}}$ Latency = 2

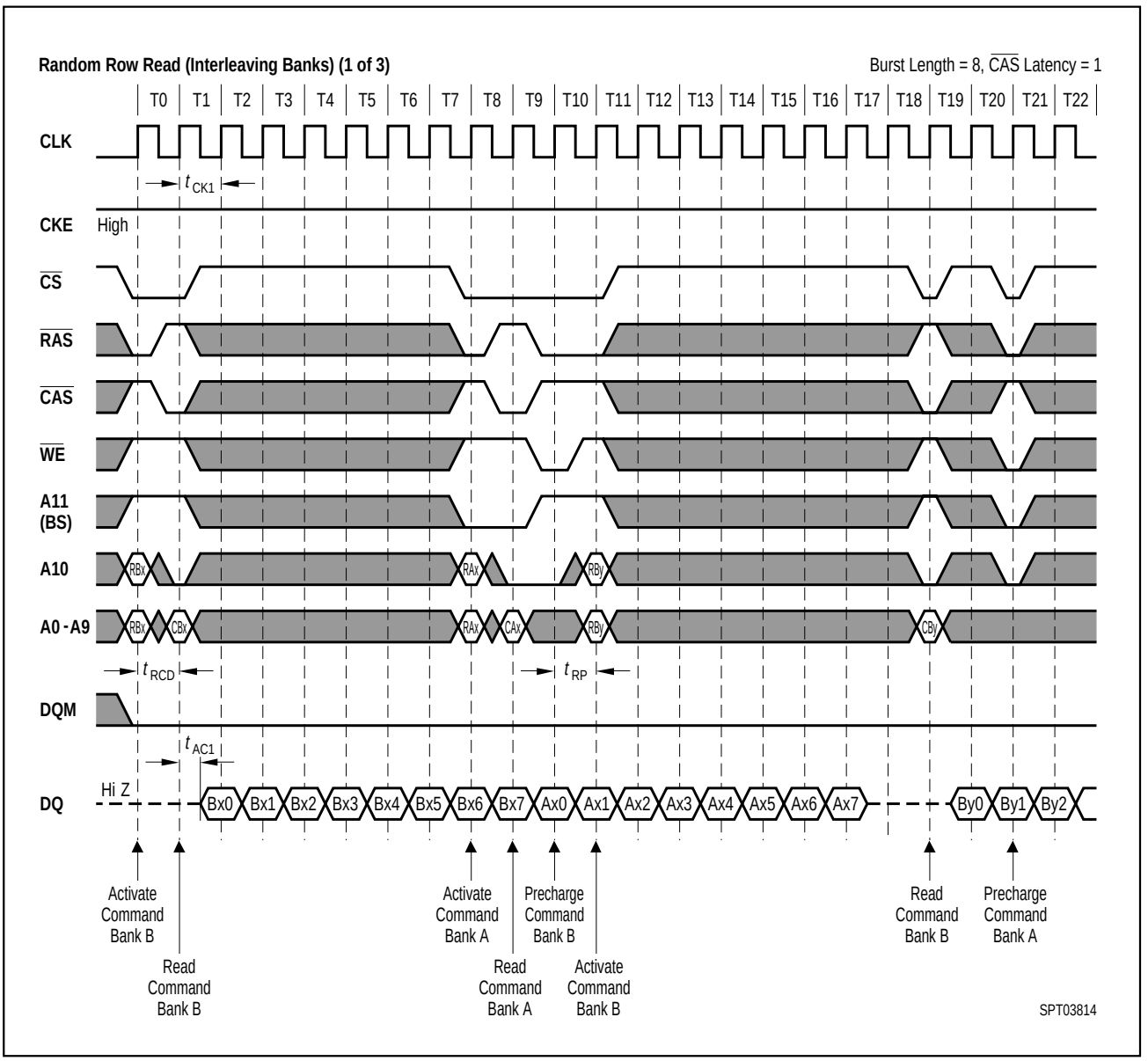


17.3. $\overline{\text{CAS}}$ Latency = 3

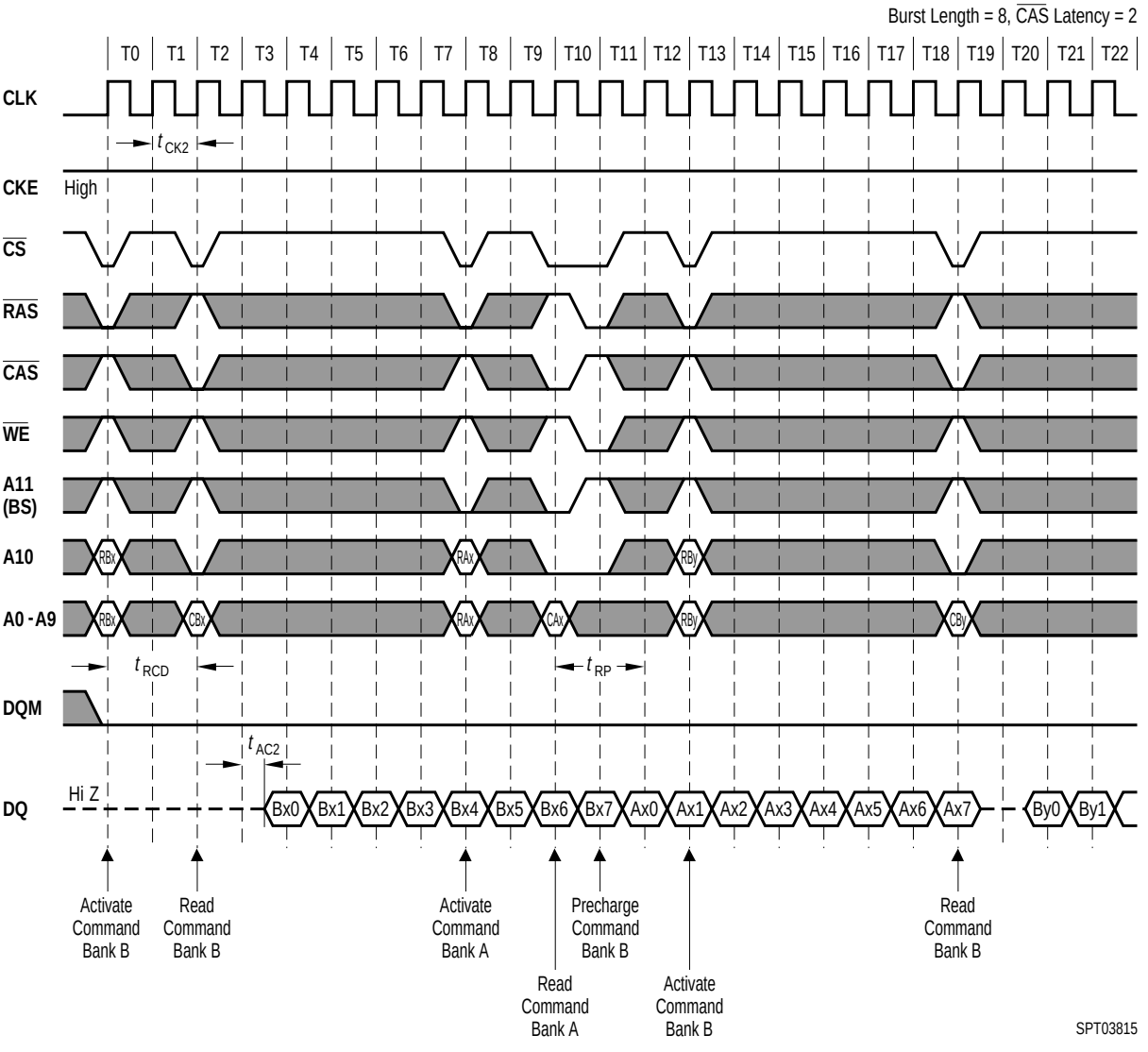


18. Random Row Read (Interleaving Banks) with Precharge

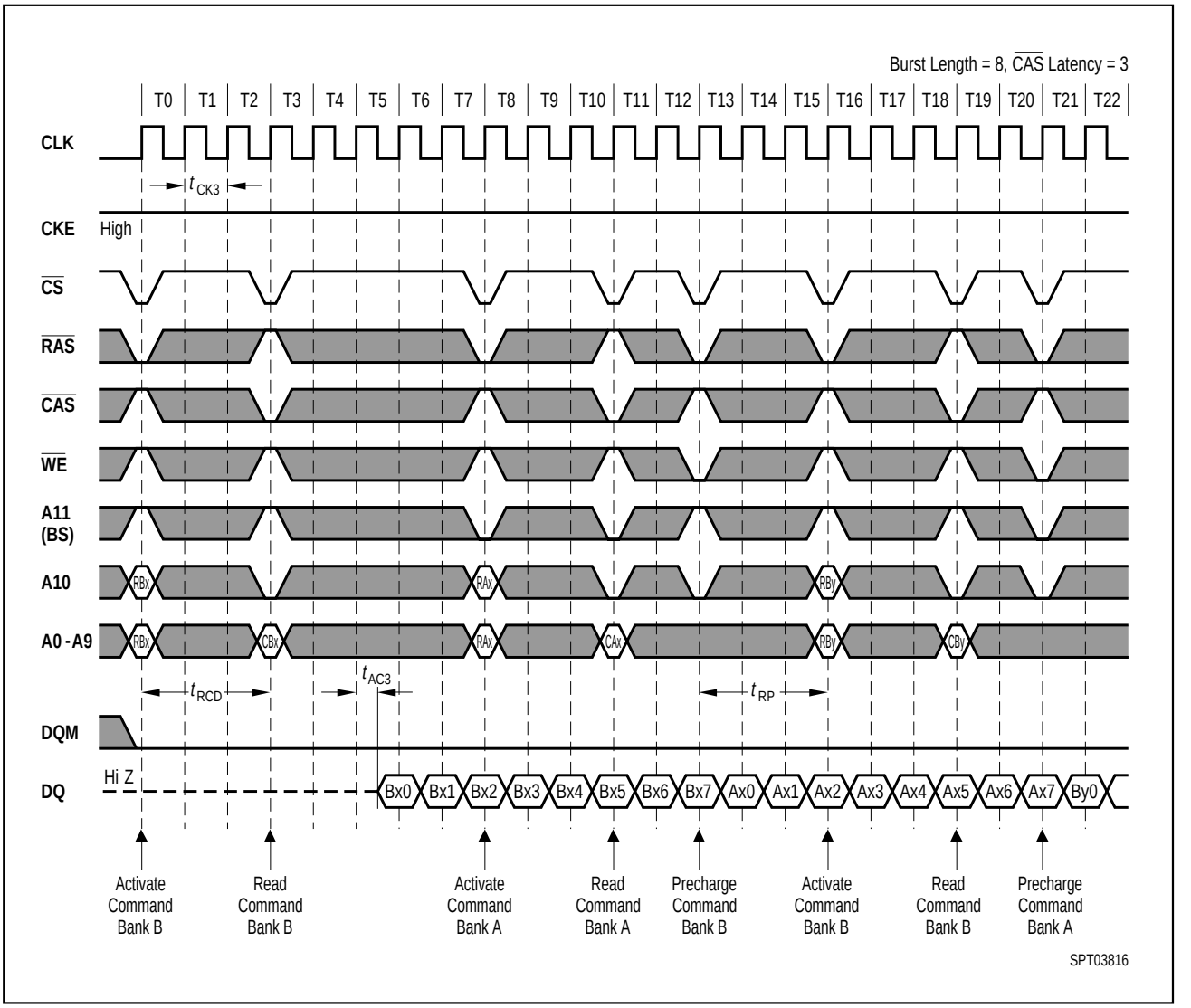
18.1. $\overline{CAS}$ Latency = 1



18.2. $\overline{\text{CAS}}$ Latency = 2

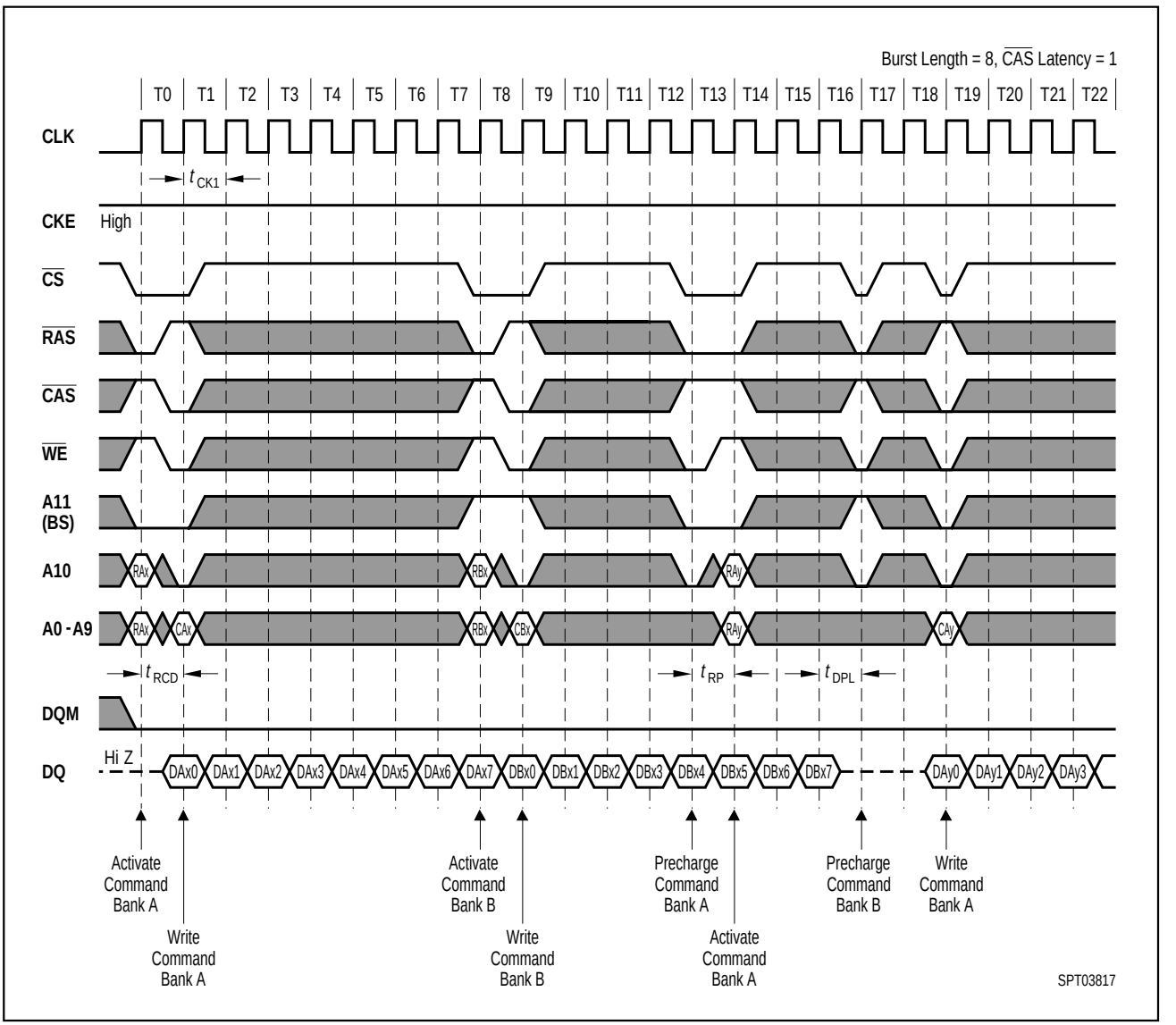


18.3. $\overline{\text{CAS}}$ Latency = 3

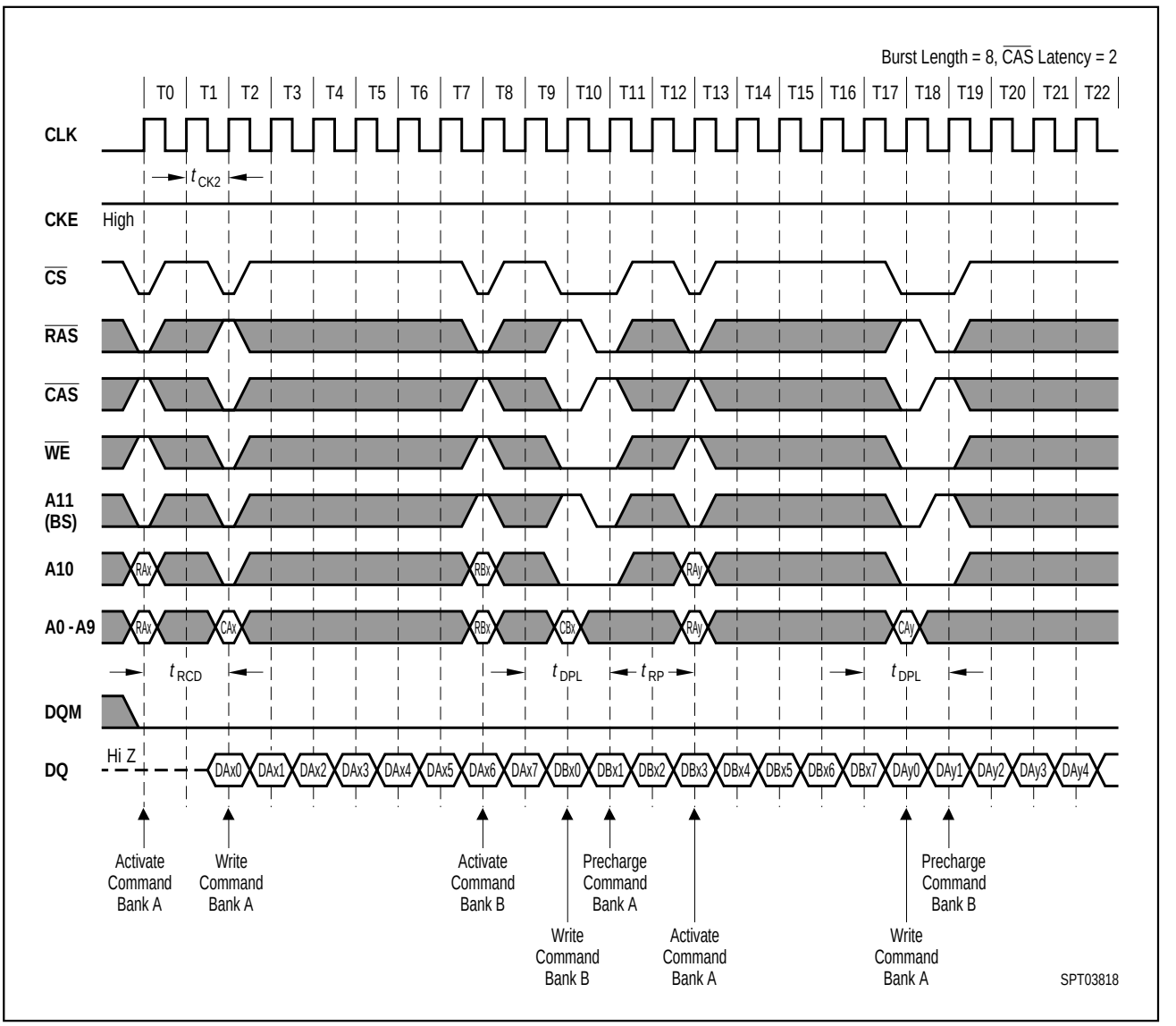


19. Random Row Write (Interleaving Banks) with Precharge

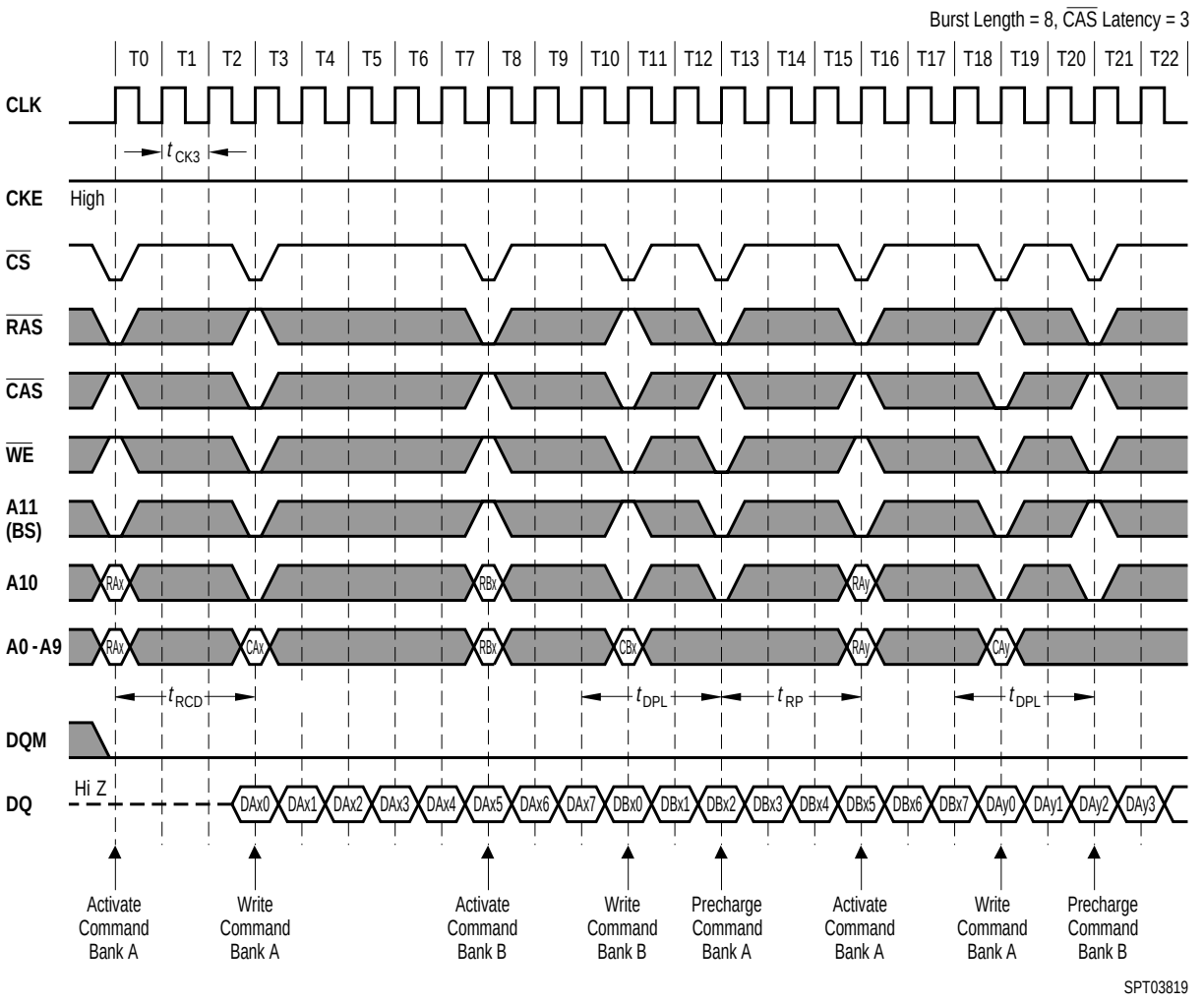
19.1. $\overline{CAS}$ Latency = 1



19.2. $\overline{\text{CAS}}$ Latency = 2

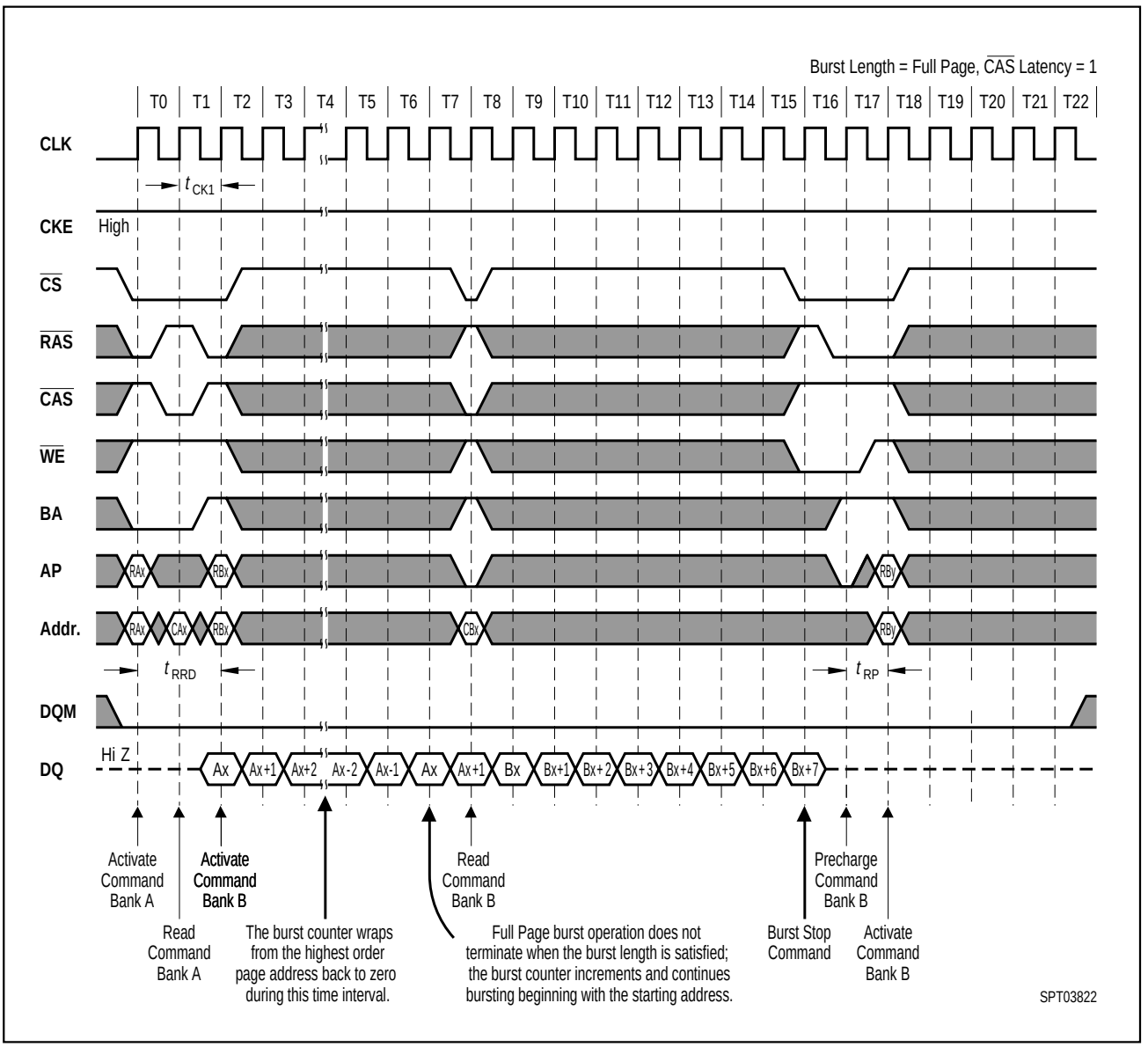


19.3. $\overline{CAS}$ Latency = 3

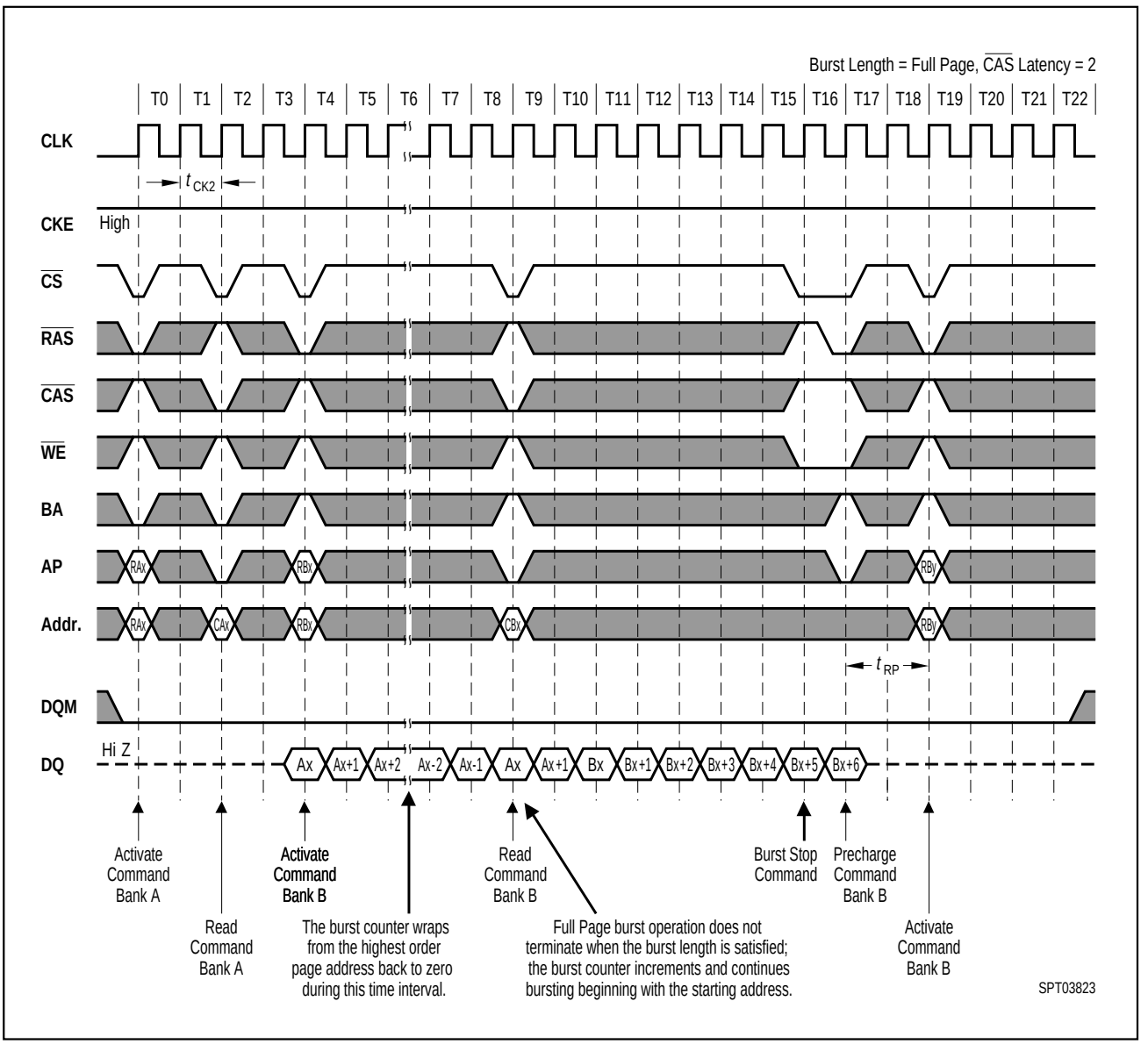


20. Full Page Read Cycle

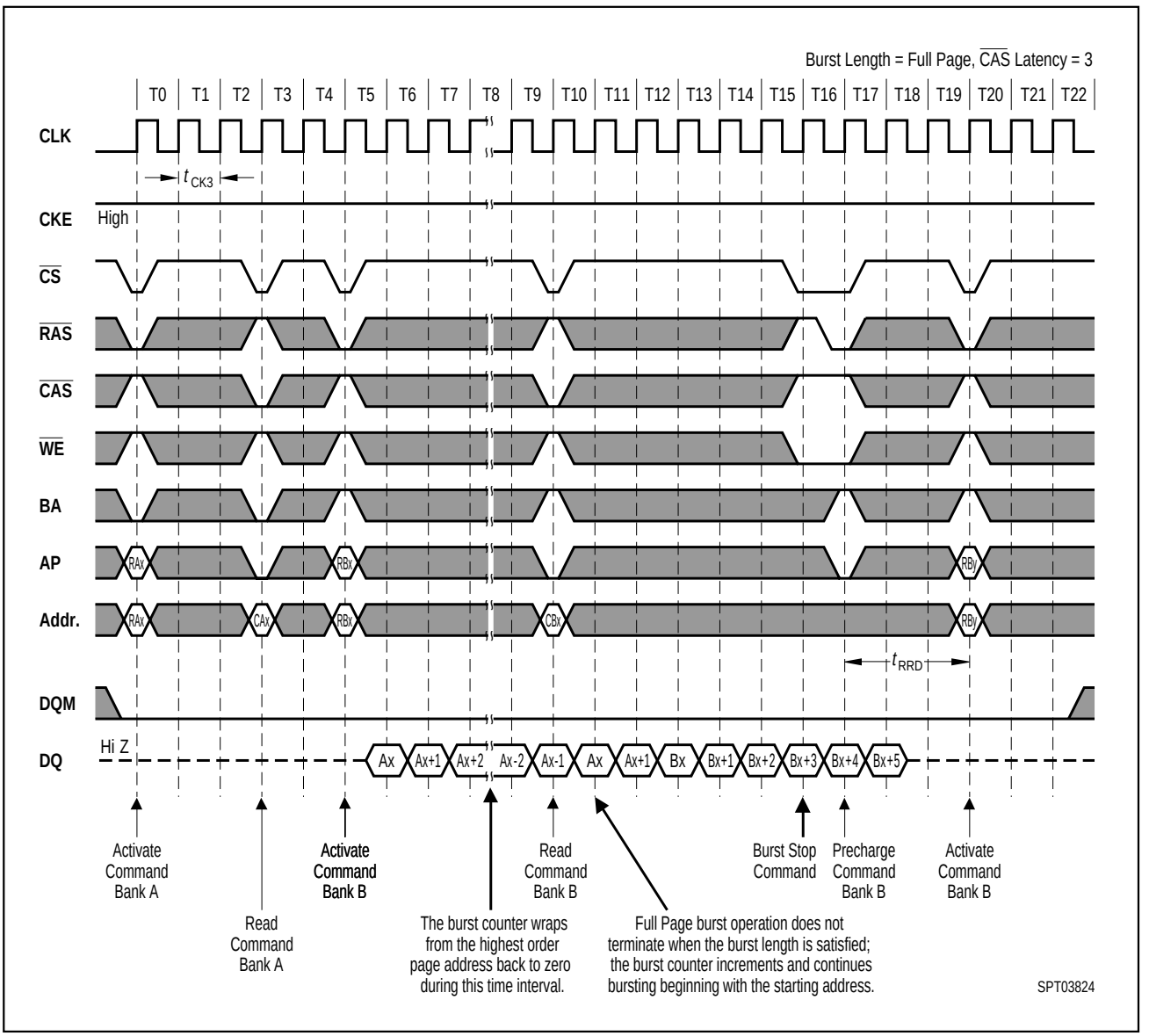
20.1. $\overline{CAS}$ Latency = 1



20.2. $\overline{CAS}$ Latency = 2

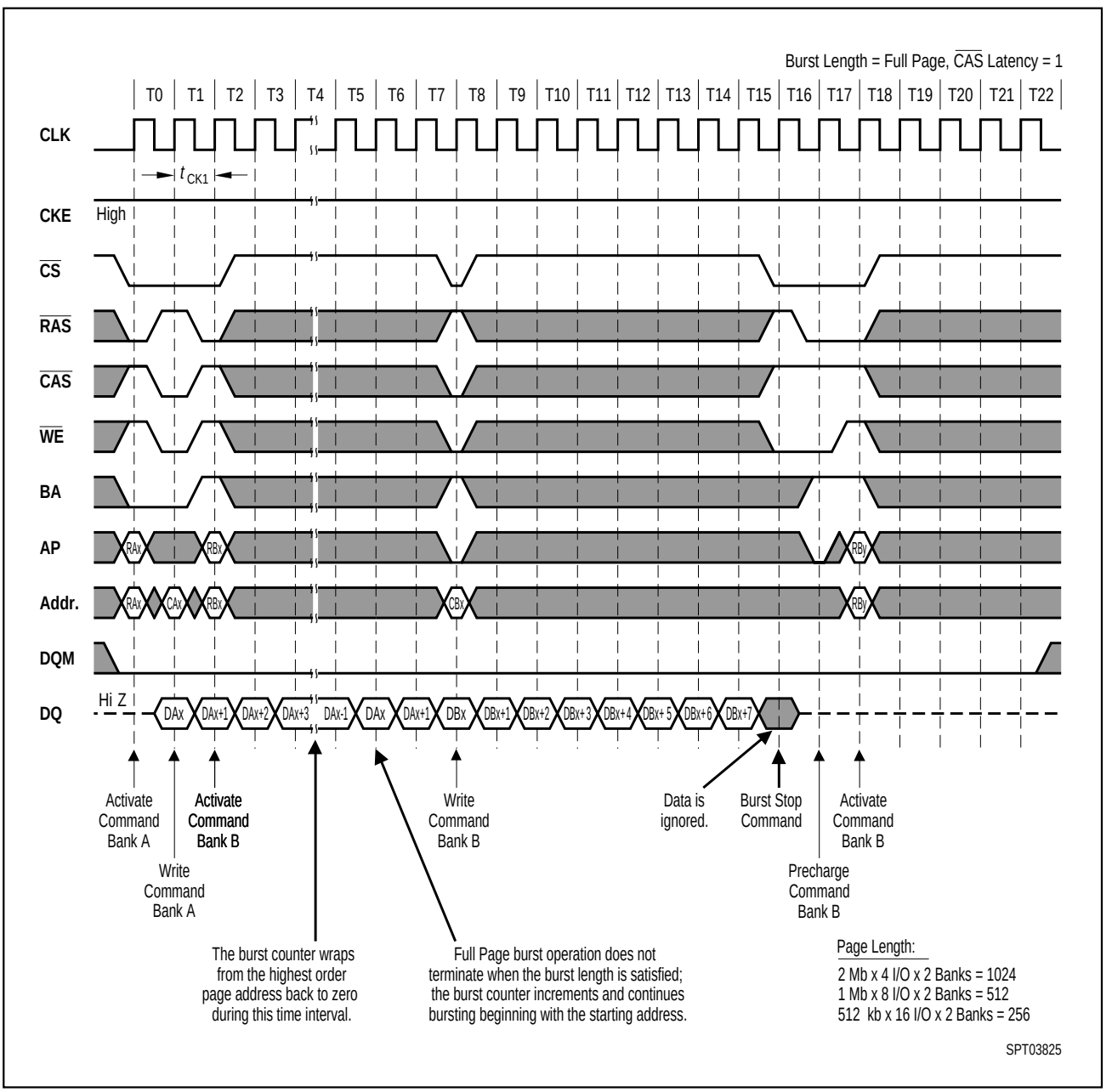


20.3. $\overline{\text{CAS}}$ Latency = 3

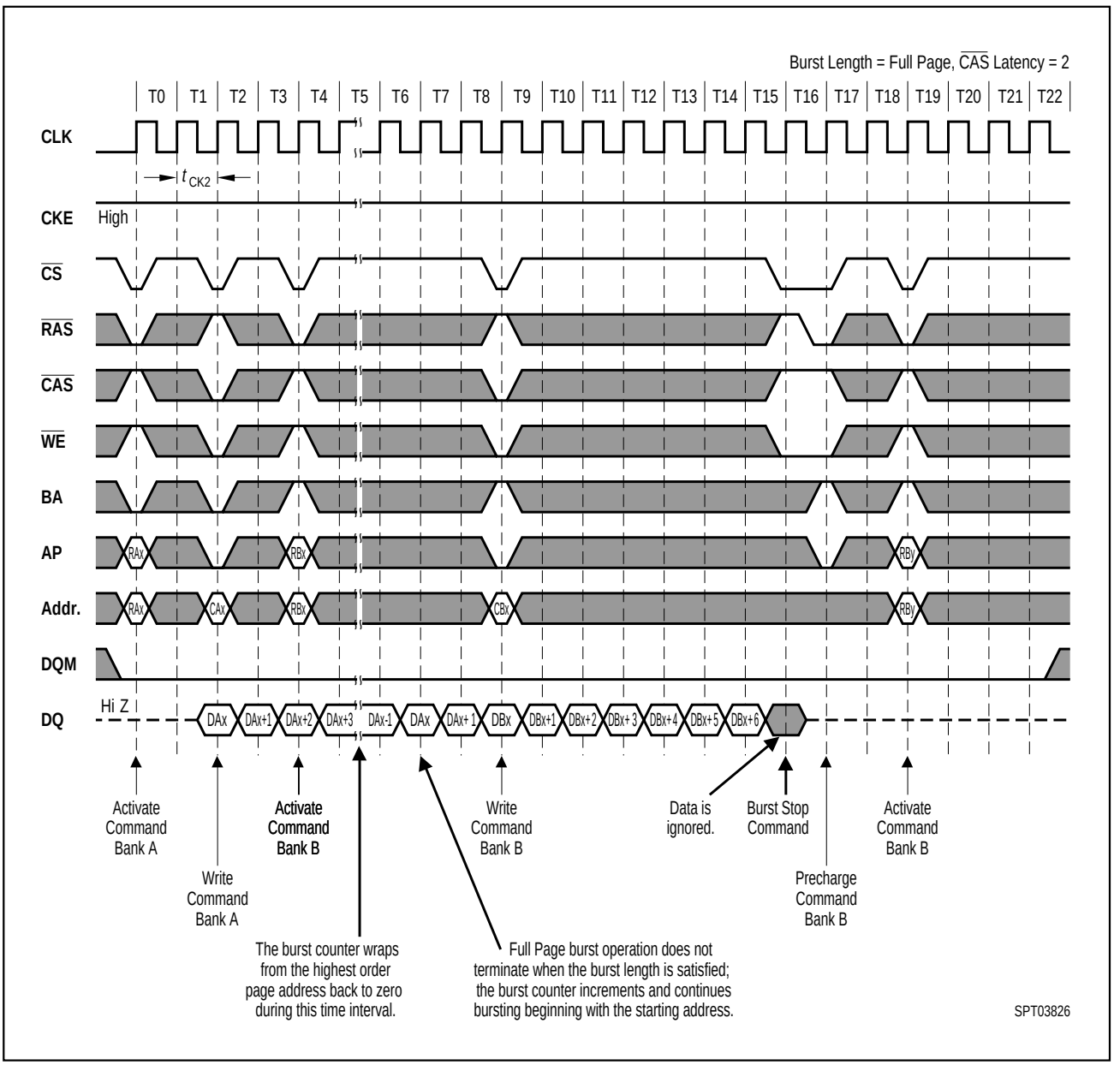


21. Full Page Write Cycle

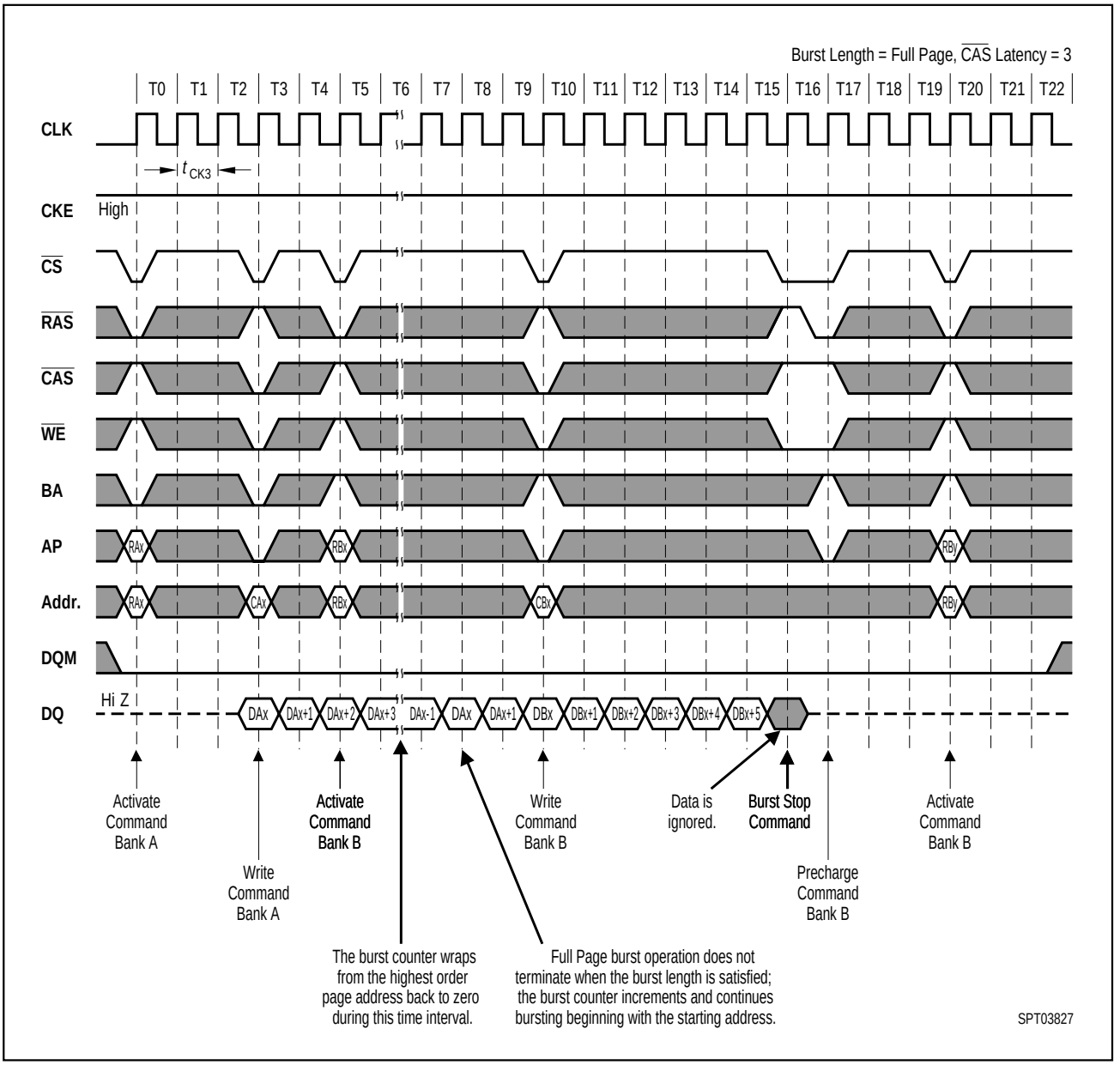
21.1. $\overline{CAS}$ Latency = 1



21.2. $\overline{CAS}$ Latency = 2

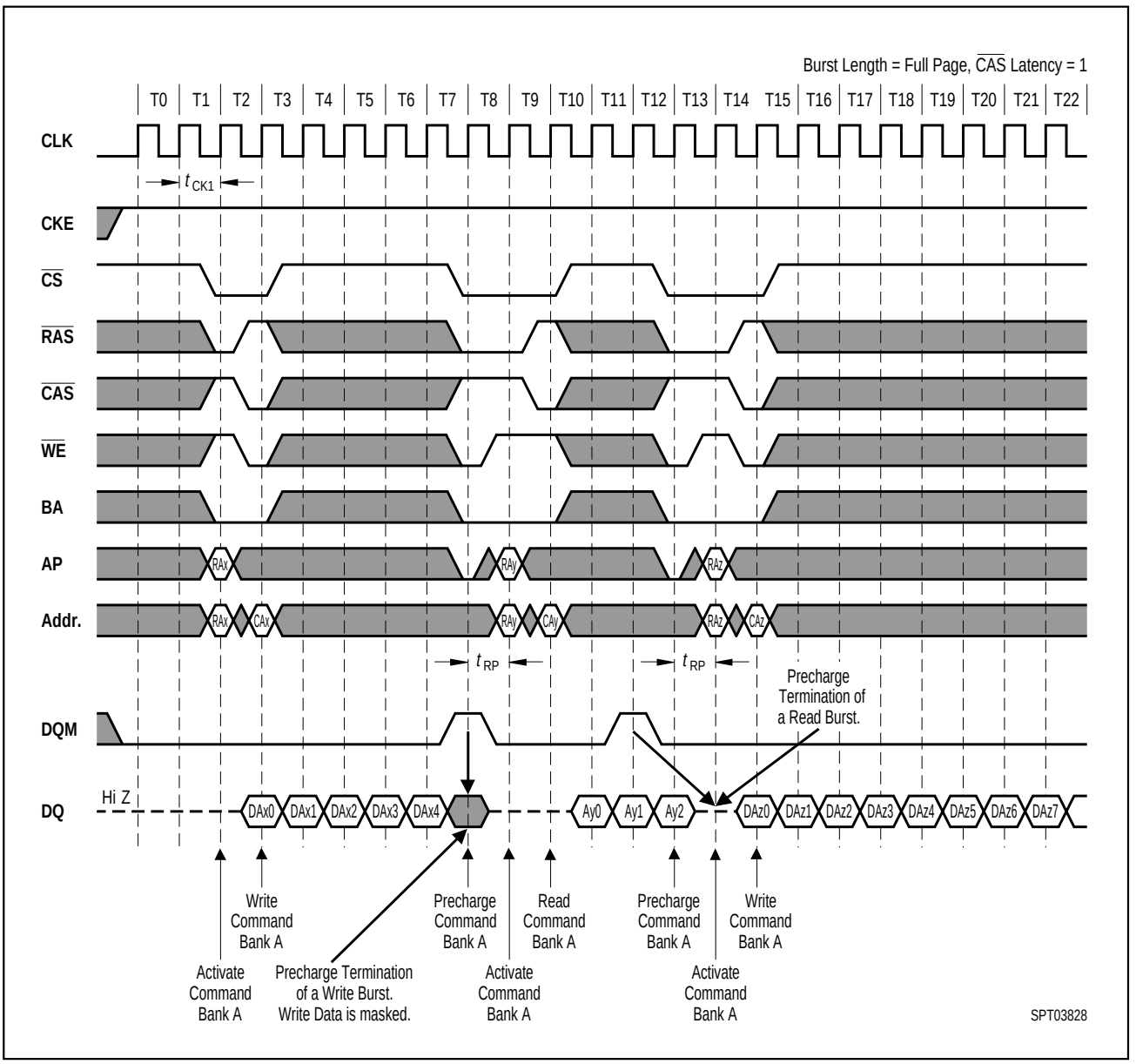


21.3. $\overline{\text{CAS}}$ Latency = 3

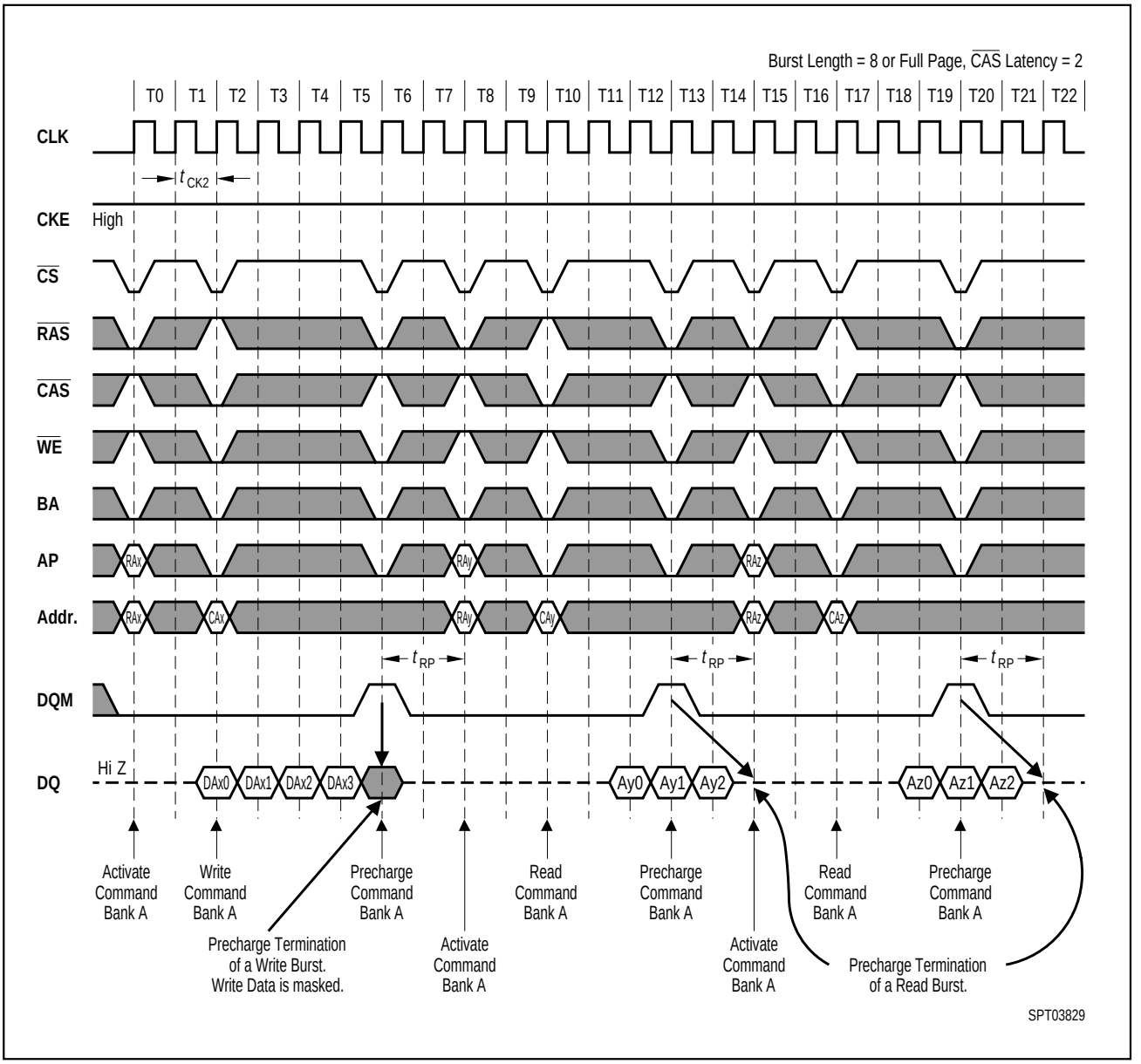


22. Precharge Termination of a Burst

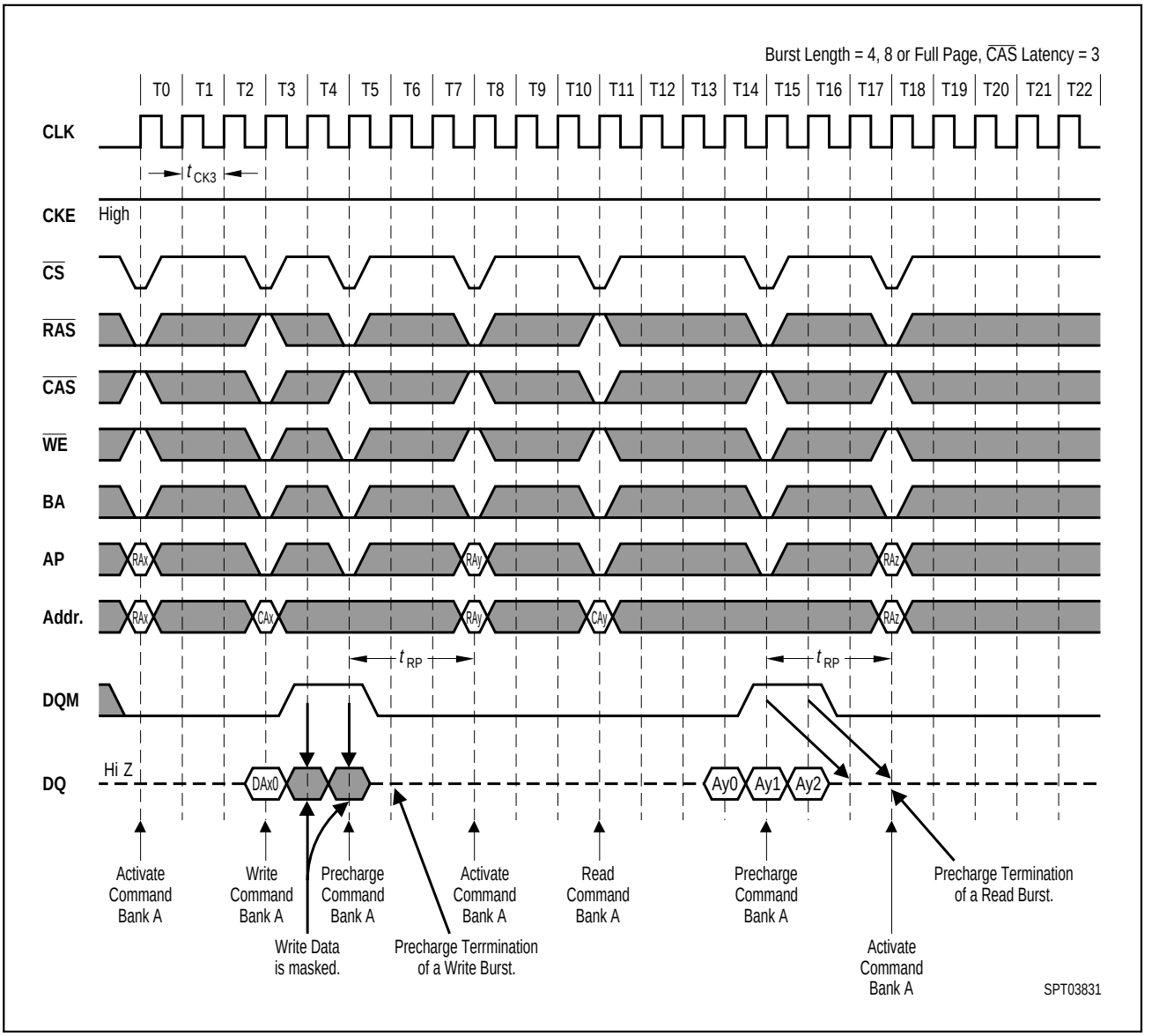
22.1. $\overline{CAS}$ Latency = 1



22.2. $\overline{\text{CAS}}$ Latency = 2



22.3. $\overline{CAS}$ Latency = 3



Complete List of Operation Commands

SDRAM Function Truth Table

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS	Addr	Action
Idle	H	X	X	X	X	X	NOP or Power Down
	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	RA	Row (&Bank) Active; Latch Row Address
	L	L	H	L	BS	AP	NOP[4]
	L	L	L	H	X	X	Auto Refresh or Self Refresh[5]
	L	L	L	L	Op-	Code	Mode reg. Access[5]
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BS	CA,AP	Begin Read; Latch CA; DetermineAP
	L	H	L	L	BS	CA,AP	Begin Write; Latch CA; DetermineAP
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, New Read, DetermineAP[3]
	L	H	L	L	BS	CA,AP	Term Burst, Start Write, DetermineAP[3]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Term Burst, Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, Start Read, DetermineAP[3]
	L	H	L	L	BS	CA,AP	Term Burst, New Write, DetermineAP[3]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	Term Burst, Precharge[3]
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	H	BS	X	ILLEGAL[2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL

SDRAM Function Truth Table (cont'd)

Current State[1]	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BS	Addr	Action
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	H	BS	X	ILLEGAL[2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Precharging	H	X	X	X	X	X	NOP;> Idle after t_{RP}
	L	H	H	H	X	X	NOP;> Idle after t_{RP}
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	NOP[4]
	L	L	L	X	X	X	ILLEGAL
Row Activating	H	X	X	X	X	X	NOP;> Row Active after t_{RCD}
	L	H	H	H	X	X	NOP;> Row Active after t_{RCD}
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Write Recovering	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL[2]
	L	H	L	X	BS	X	ILLEGAL[2]
	L	L	H	H	BS	X	ILLEGAL[2]
	L	L	H	L	BS	AP	ILLEGAL[2]
	L	L	L	X	X	X	ILLEGAL
Refreshing	H	X	X	X	X	X	NOP;> Idle after t_{RC}
	L	H	H	X	X	X	NOP;> Idle after t_{RC}
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Register Accessing	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

Clock Enable (CKE) Truth Table

STATE(n)	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	ACTION
Self-Refresh [6]	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self Refresh, Idle after t_{RC}
	L	H	L	H	H	H	X	EXIT Self Refresh, Idle after t_{RC}
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power-Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Power-Down, > Idle
	L	H	L	H	H	H	X	EXIT Power-Down, > Idle
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Low-Power Mode)
All. Banks Idle [7]	H	H	X	X	X	X	X	Refer to the function truth table
	H	L	H	X	X	X	X	Enter Power-Down
	H	L	L	H	H	H	X	Enter Power-Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to the function truth table
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle[8]
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle[8]
	L	L	X	X	X	X	X	Maintain Clock Suspend

Abbreviations

RA = Row Address
BS = Bank Address
CA = Column Address
AP = Auto Precharge

Notes for SDRAM Function Truth Table

1. Current State is state of the bank determined by BS. All entries assume that $\overline{CKE}$ was active (HIGH) during the preceding clock cycle.
2. Illegal to bank in specified state; function may be legal in the bank indicated by BS, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in Idle state. May precharge bank(s) indicated by BS (and AP).
5. Illegal if any bank is not Idle.
6. $\overline{CKE}$ Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power-Down and Self Refresh can be entered only from the All Banks Idle State.
8. Must be legal command as defined in the SDRAM function truth table.